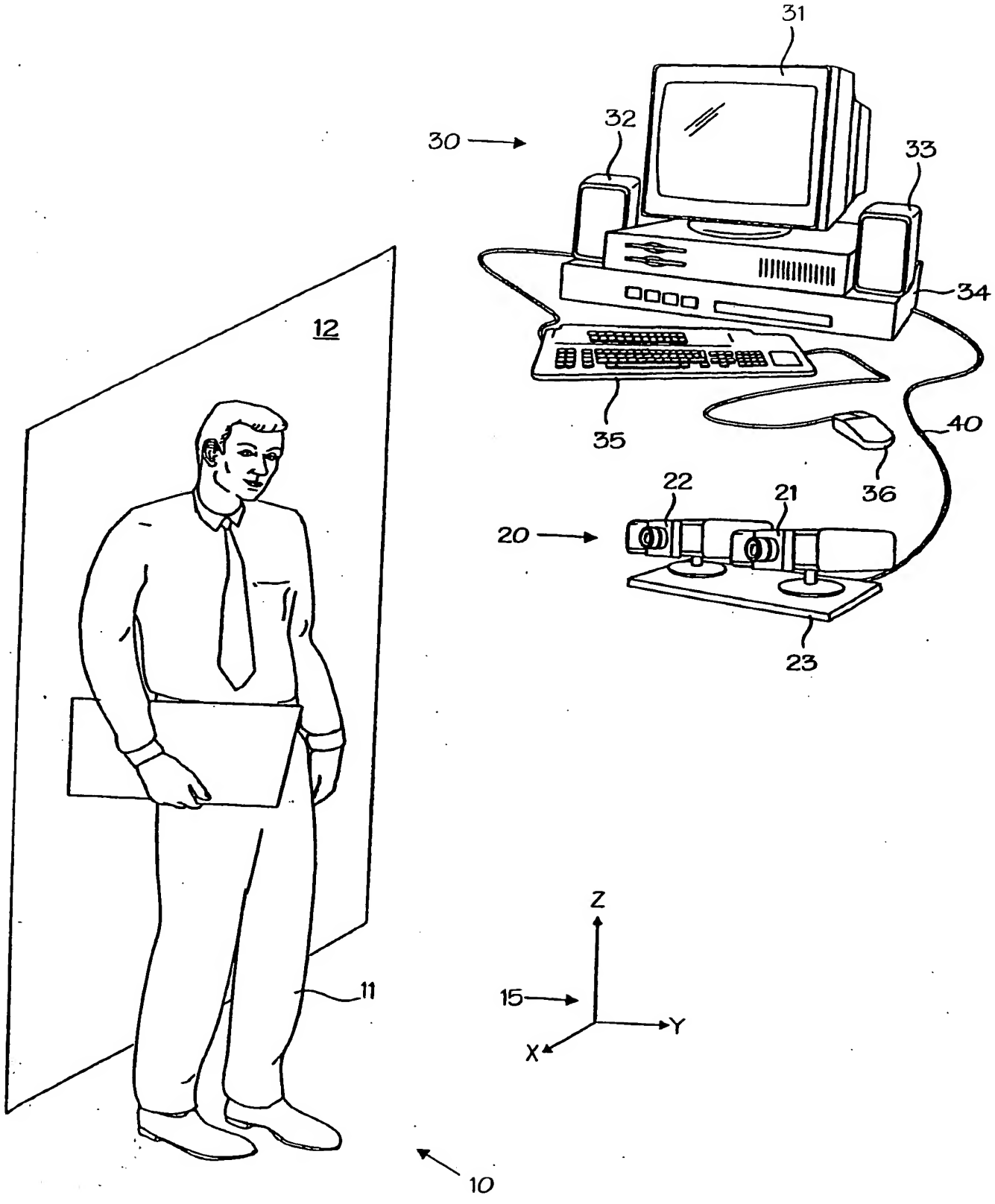

FIG. 1

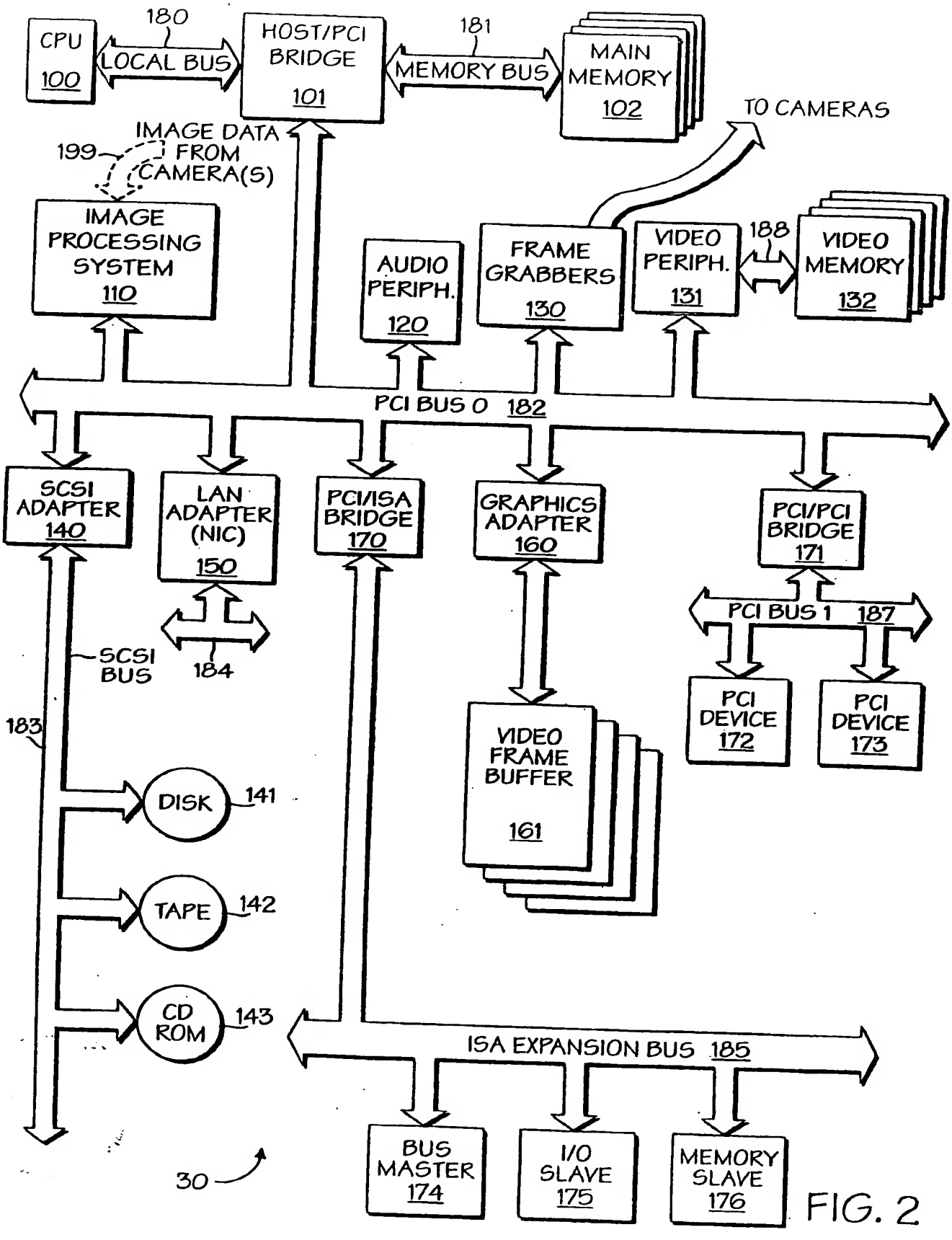
CPU
100
180
LOCAL BUS
HOST/PCI
BRIDGE
101
181
MEMORY BUS
MAIN
MEMORY
102
TO CAMERAS
IMAGE DATA
FROM
CAMERA(S)
199
IMAGE
PROCESSING
SYSTEM
110
AUDIO
PERIPH.
120
FRAME
GRABBERS
130
VIDEO
PERIPH.
131
188
VIDEO
MEMORY
132
PCI BUS 0 182
SCSI
ADAPTER
140
LAN
ADAPTER
(NIC)
150
PCI/ISA
BRIDGE
170
GRAPHICS
ADAPTER
160
PCI/PCI
BRIDGE
171
PCI BUS 1 187
SCSI
BUS
184
183
PCI
DEVICE
172
PCI
DEVICE
173
VIDEO
FRAME
BUFFER
161
DISK
141
TAPE
142
CD
ROM
143
ISA EXPANSION BUS 185
BUS
MASTER
174
I/O
SLAVE
175
MEMORY
SLAVE
176
30

FIG. 2

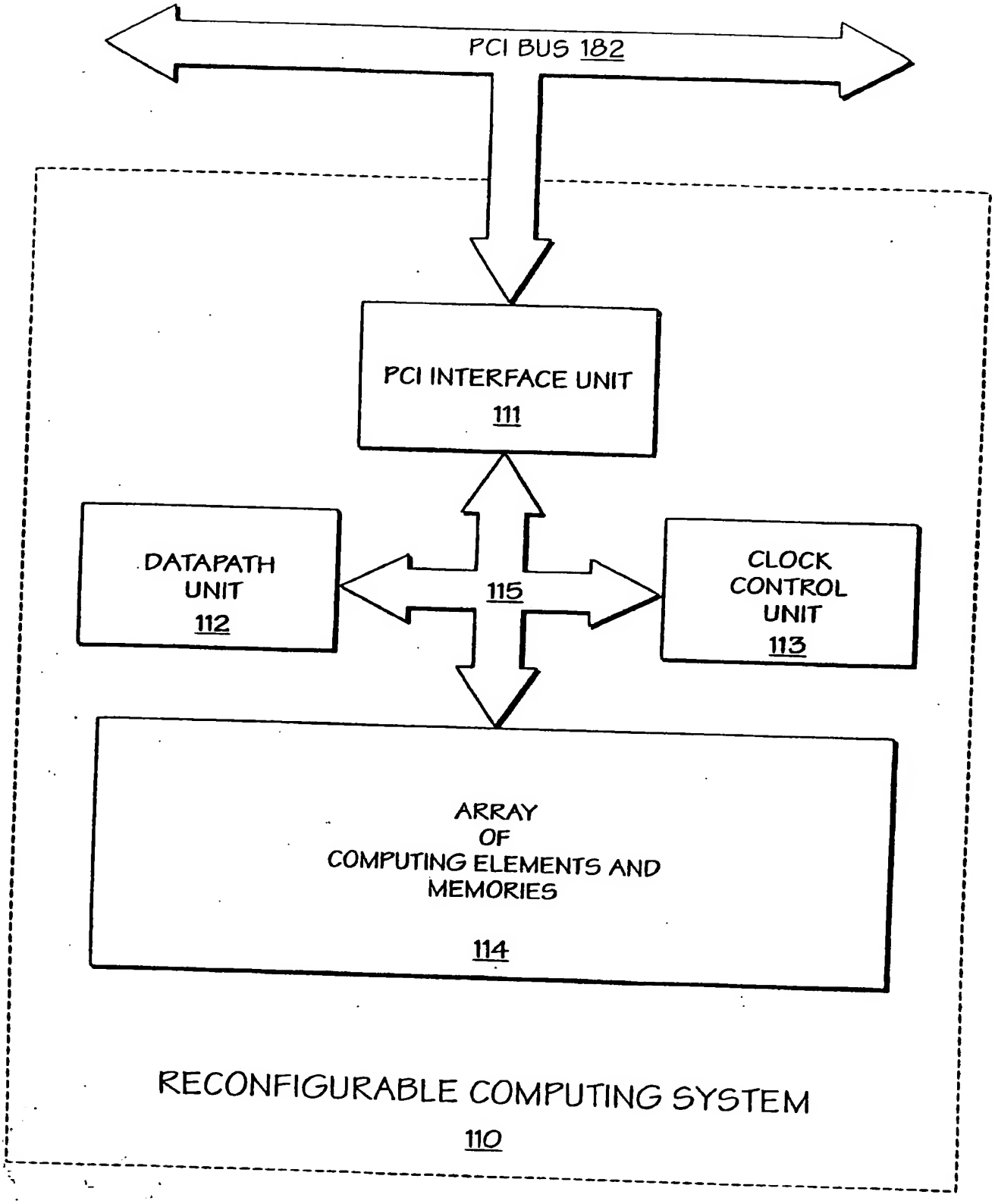
PCI BUS 182
PCI INTERFACE UNIT
111
DATAPATH
UNIT
112
115
CLOCK
CONTROL
UNIT
113
ARRAY
OF
COMPUTING ELEMENTS AND
MEMORIES
114
RECONFIGURABLE COMPUTING SYSTEM
110

FIG. 3

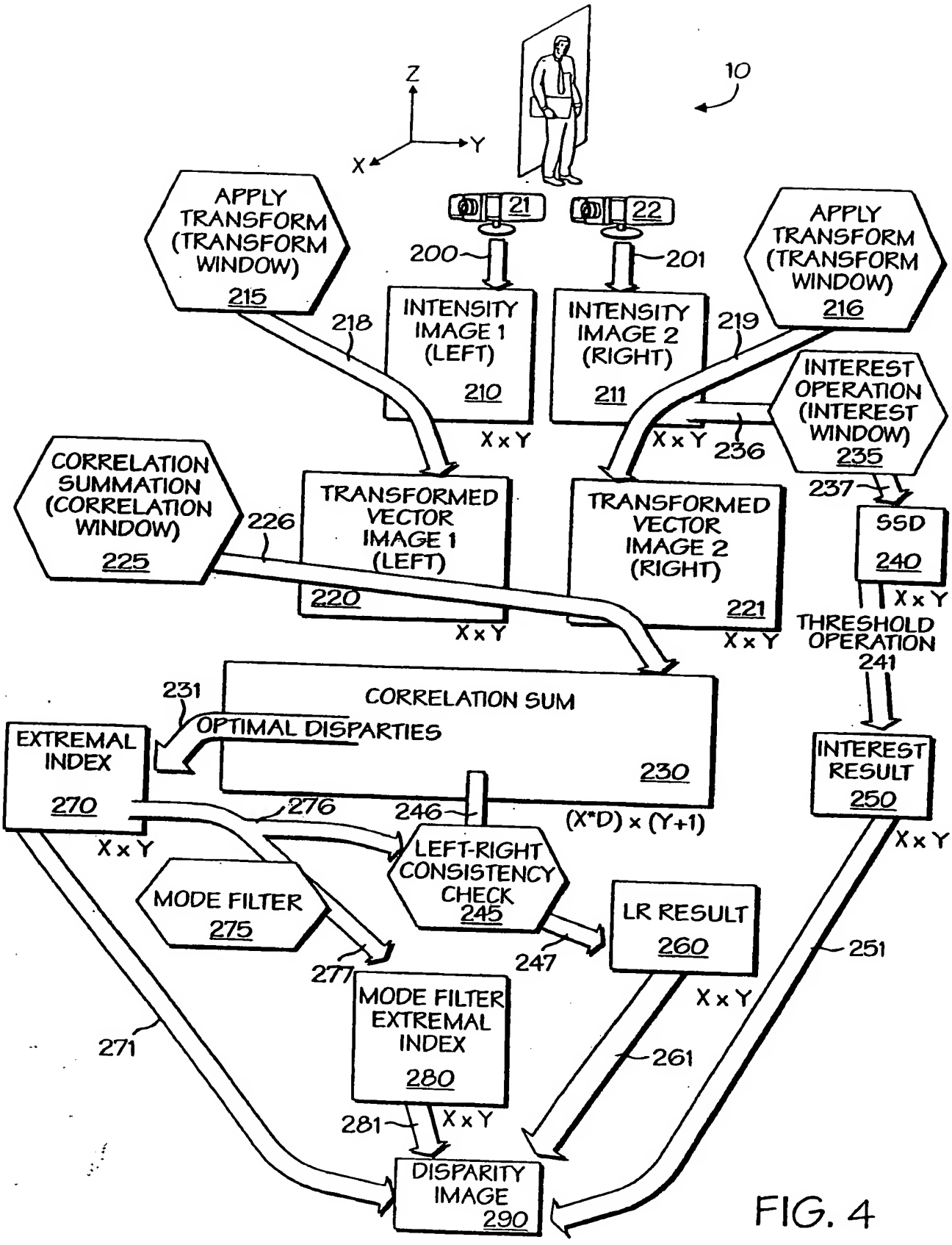
Z
Y
X
10
21
22
APPLY TRANSFORM (TRANSFORM WINDOW) 215
200
201
APPLY TRANSFORM (TRANSFORM WINDOW) 216
218
INTENSITY IMAGE 1 (LEFT) 210
INTENSITY IMAGE 2 (RIGHT) 211
219
INTEREST OPERATION (INTEREST WINDOW) 235
X x Y
X x Y
236
237
CORRELATION SUMMATION (CORRELATION WINDOW) 225
226
TRANSFORMED VECTOR IMAGE 1 (LEFT) 220
TRANSFORMED VECTOR IMAGE 2 (RIGHT) 221
SSD 240
X x Y
X x Y
X x Y
THRESHOLD OPERATION 241
231
CORRELATION SUM
OPTIMAL DISPARTIES
230
EXTREMAL INDEX 270
INTEREST RESULT 250
276
246
(X*D) x (Y+1)
X x Y
X x Y
LEFT-RIGHT CONSISTENCY CHECK 245
MODE FILTER 275
LR RESULT 260
277
247
251
MODE FILTER EXTREMAL INDEX 280
X x Y
271
261
281
X x Y
DISPARITY IMAGE 290

FIG. 4

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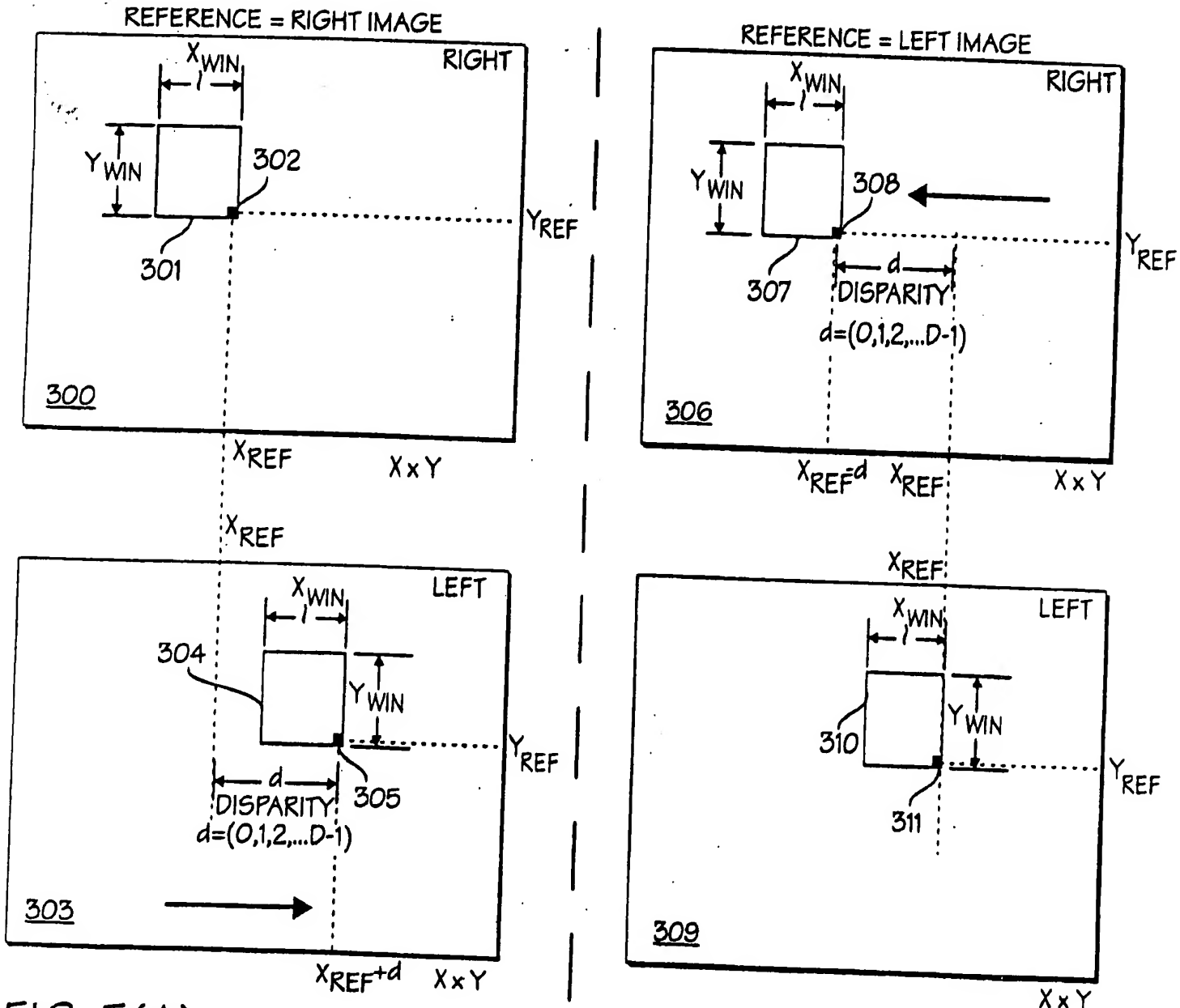


FIG. 5(A)

FIG. 5(B)

EP 1 260 940 A2

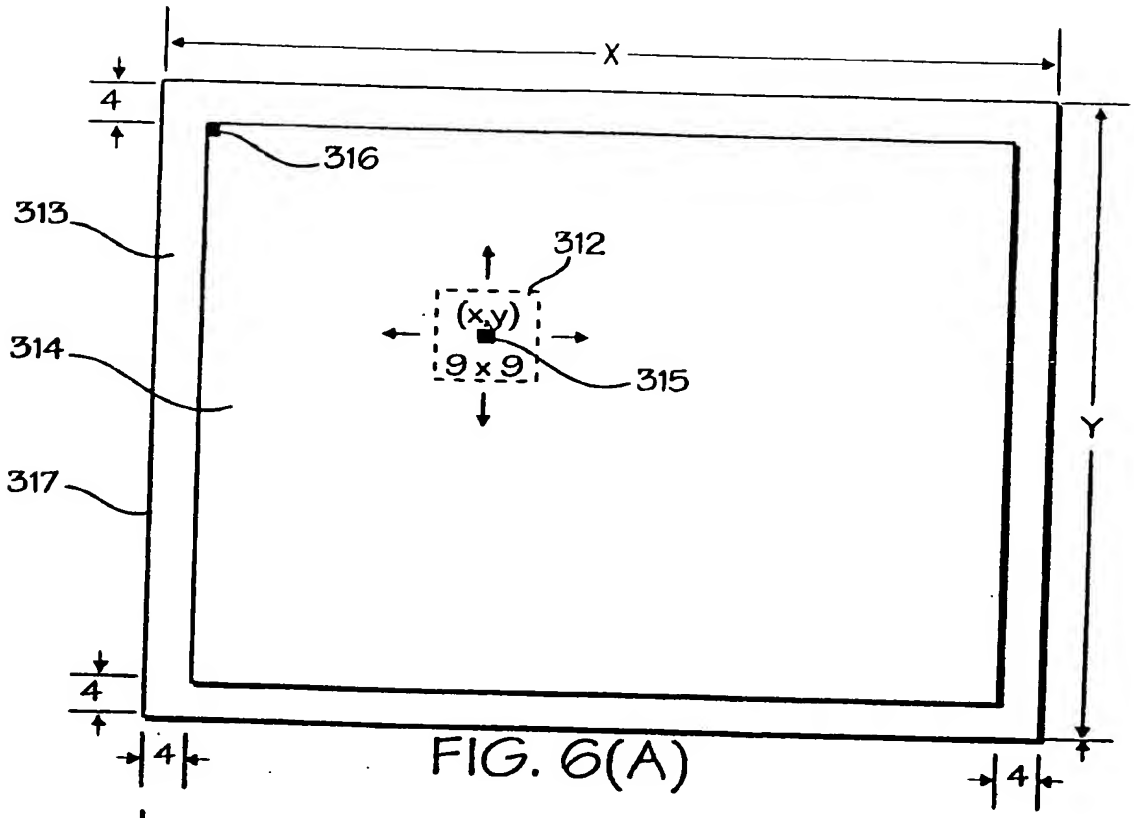


FIG. 6(A)

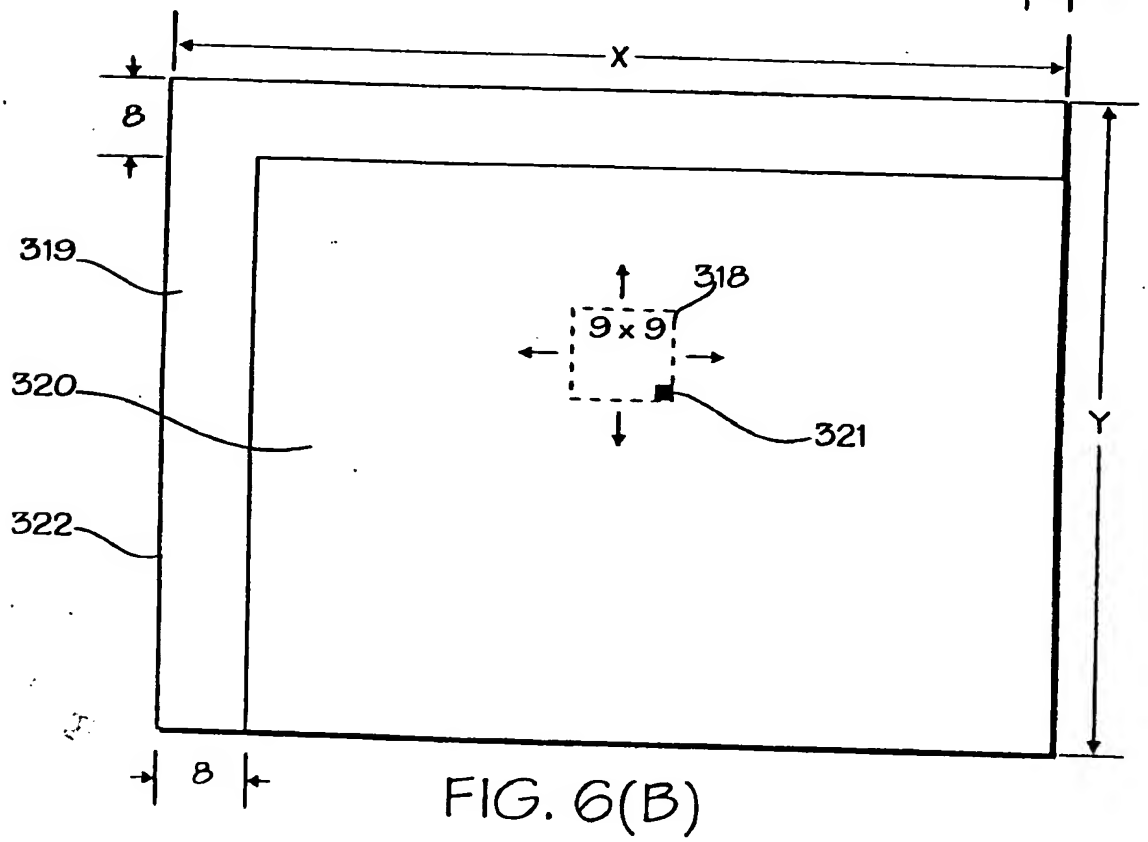


FIG. 6(B)

DATA FOR CENSUS VECTOR
CENTERED AT (x,y)

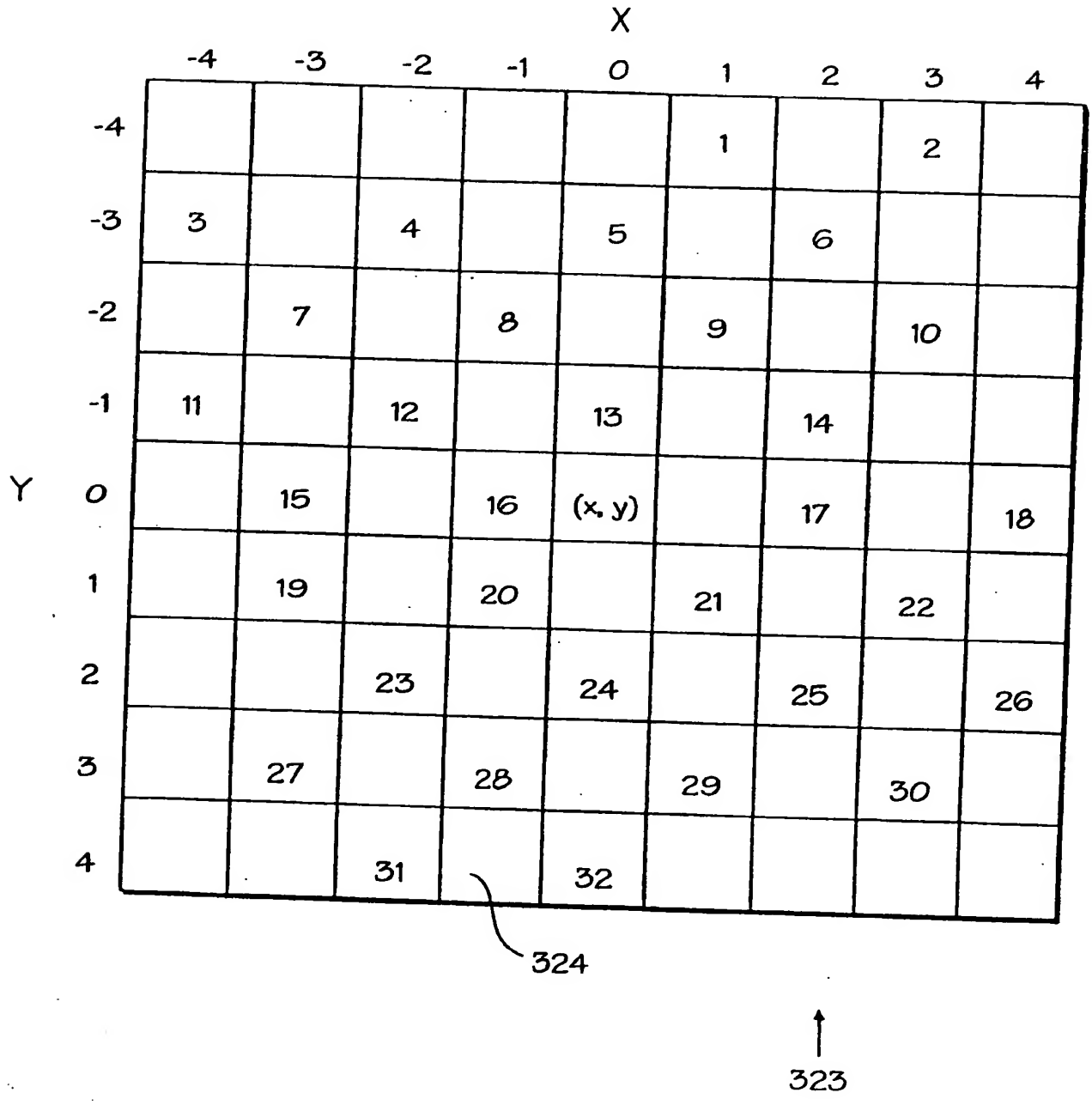


Fig. 7

Fig. 8(A)

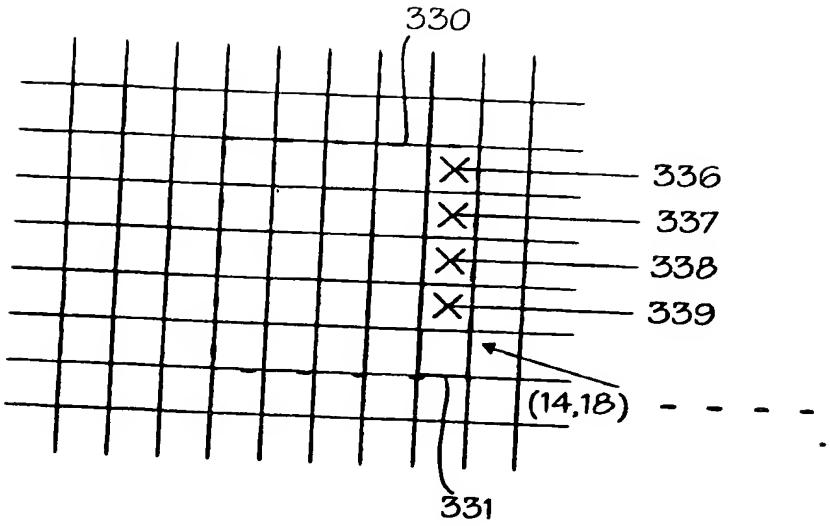


Fig. 8(B)

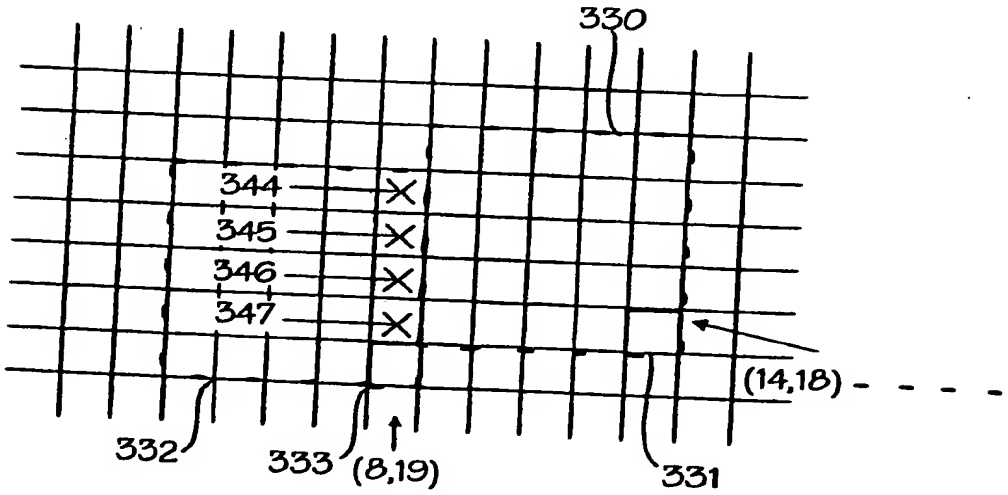


Fig. 8(C)

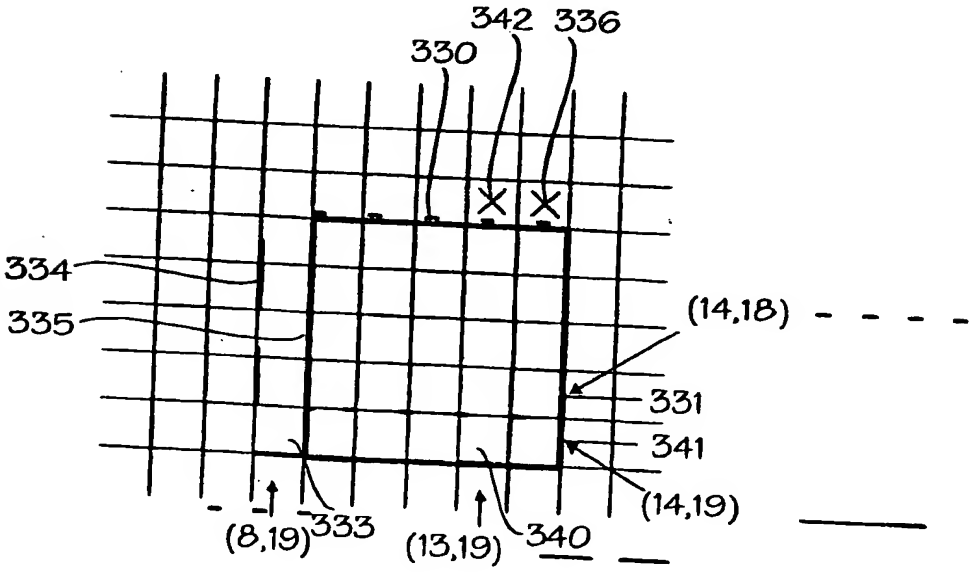


Fig. 9(A)

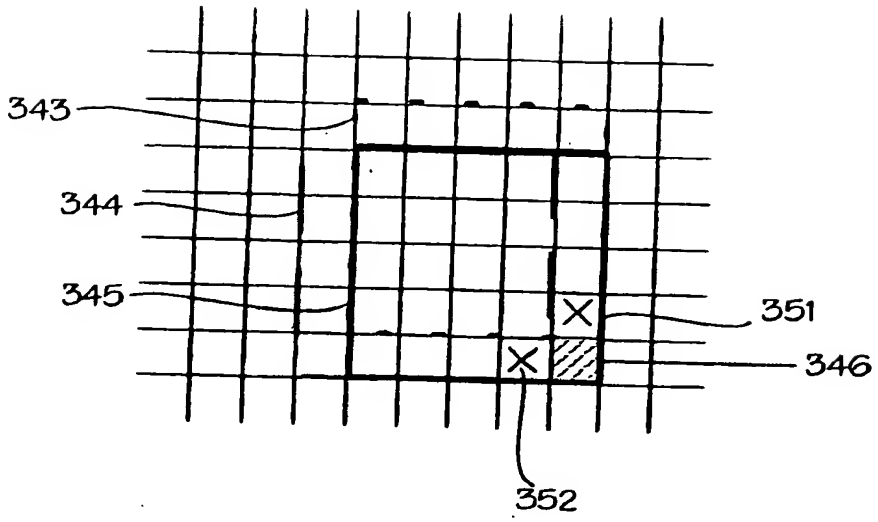


Fig. 9(B)

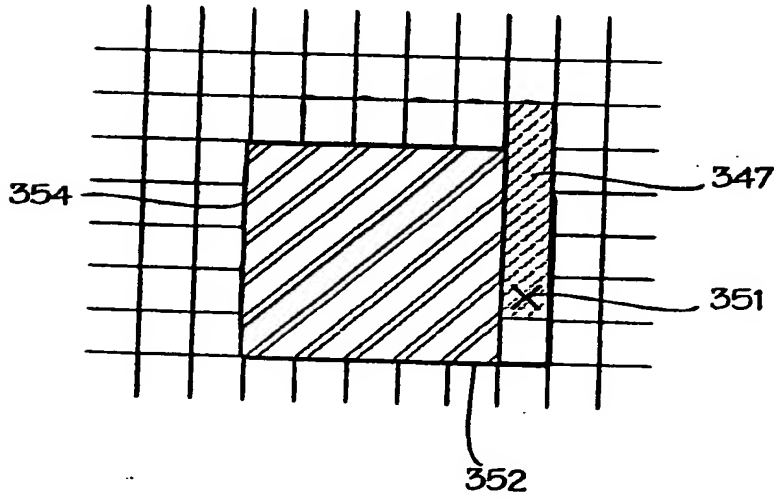
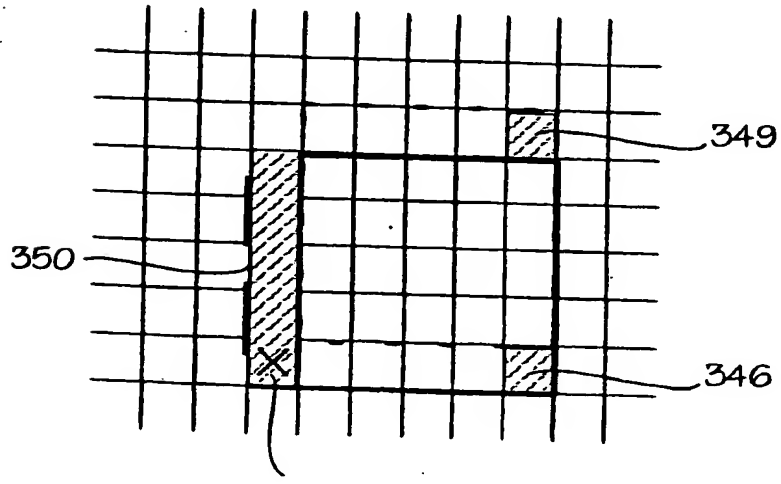


Fig. 9(C)



20120298020T

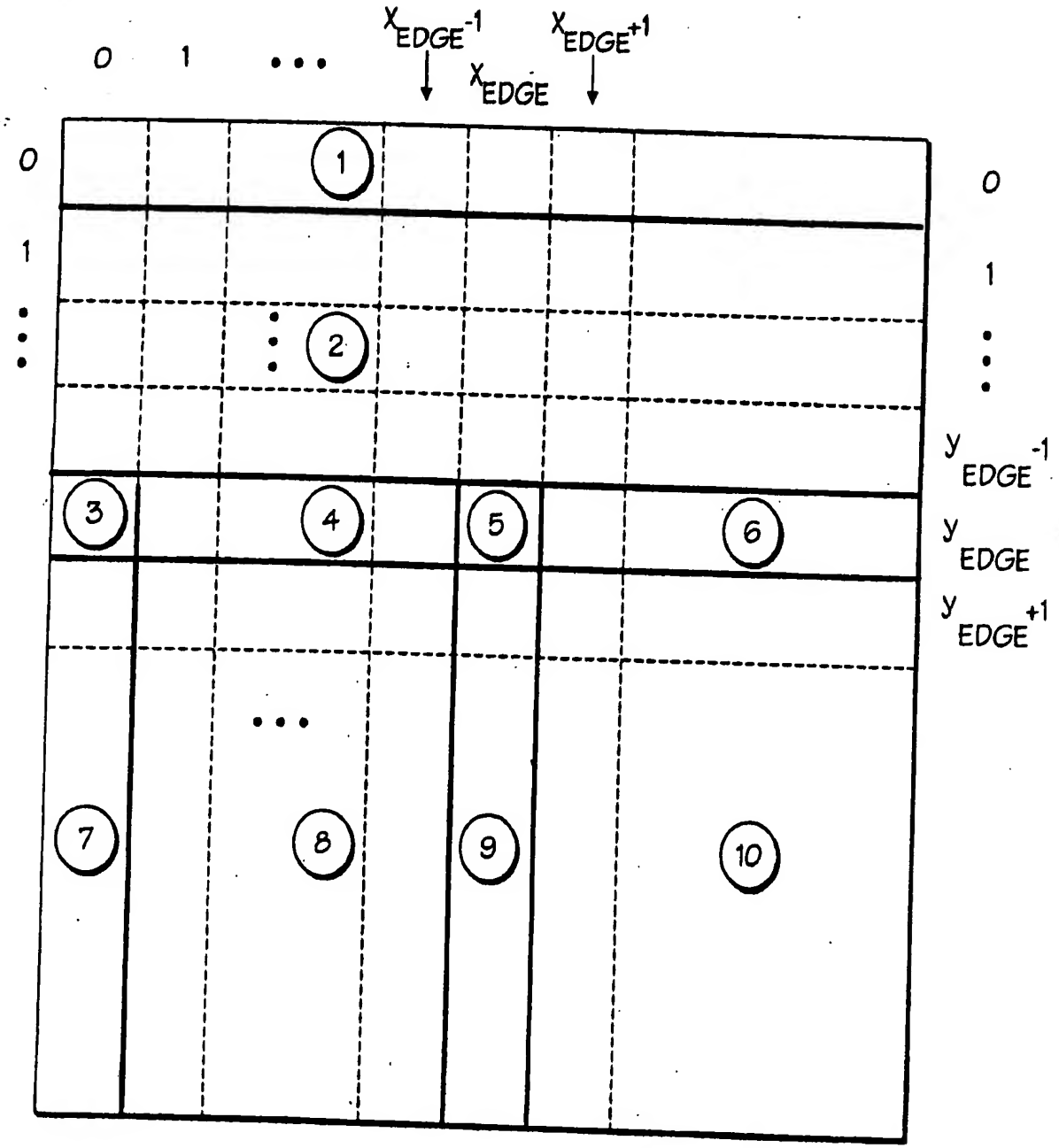


Fig. 10A

20020260 : 20030001

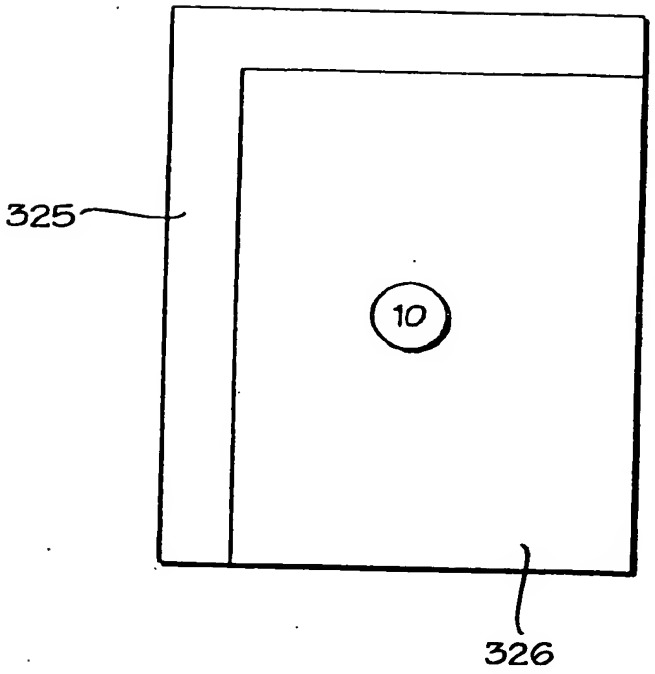


Fig. 10(B)

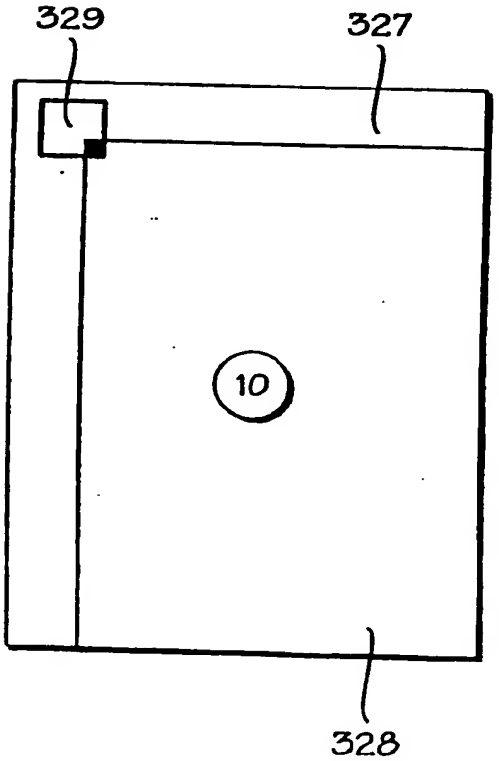


Fig. 10(C)

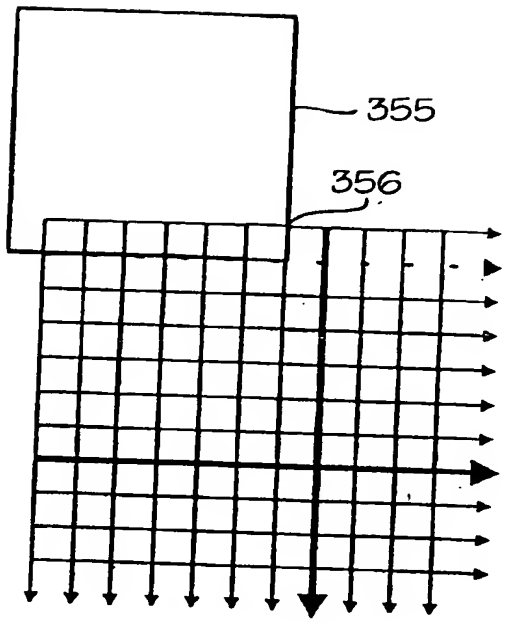


Fig. 11(A)

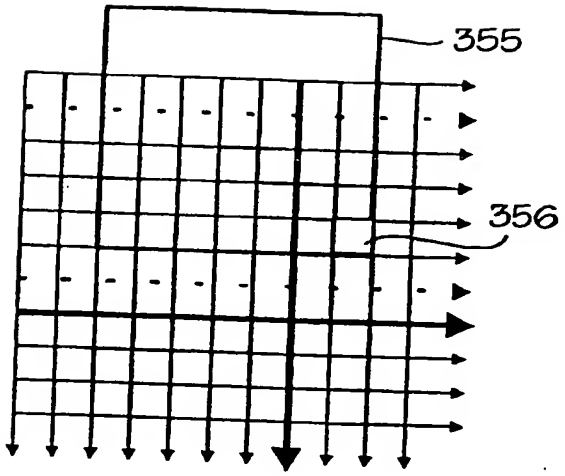


Fig. 11(B)

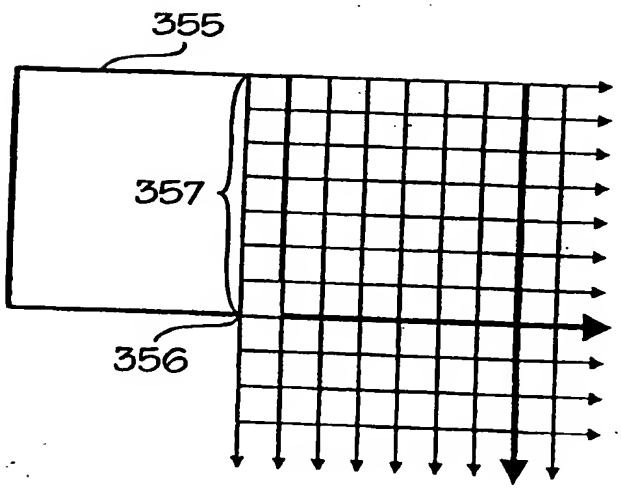


Fig. 11(C)

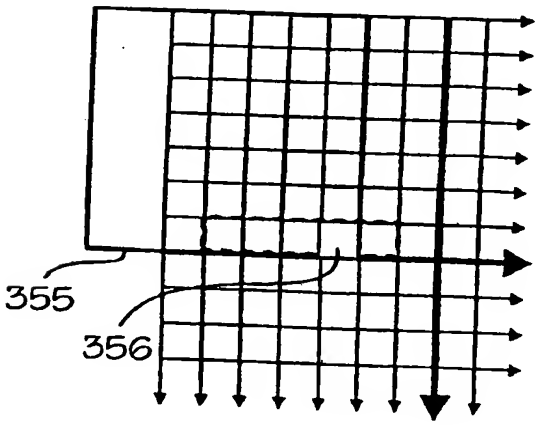


Fig. 11(D)

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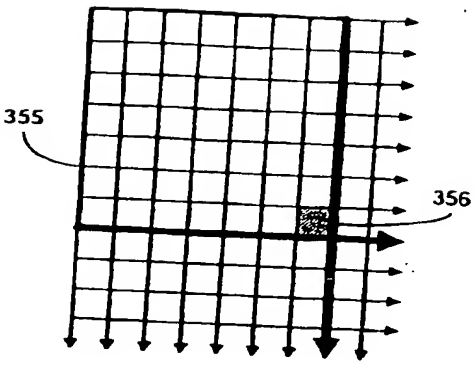


Fig. 11 (E)

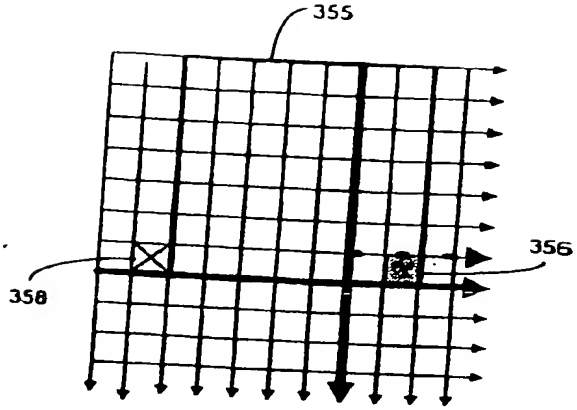


Fig. 11 (F)

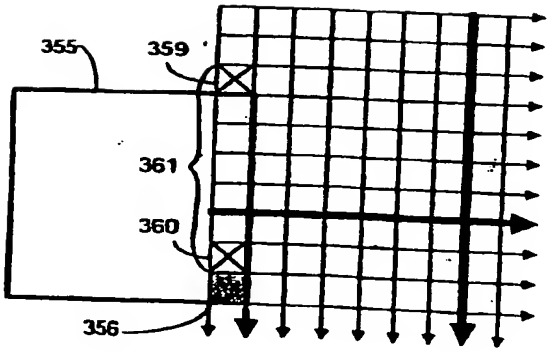


Fig. 11 (G)

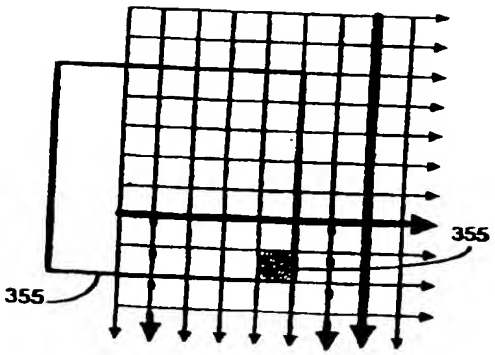


Fig. 11 (H)

20120260 - 25-06-2007

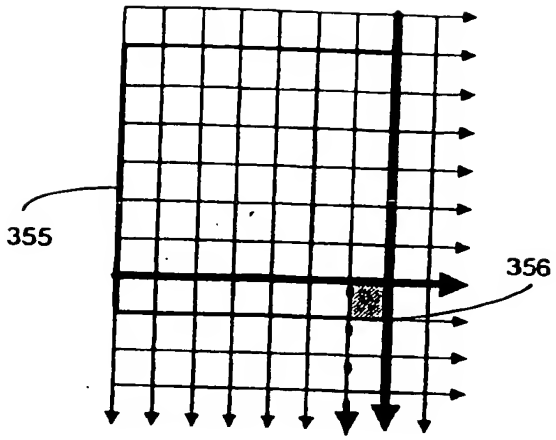


Fig. 11 (I)

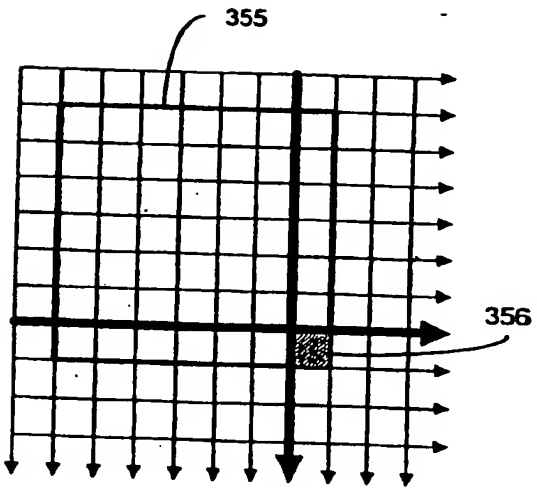


Fig. 11 (J)

EP 1 672 926 A2 - 21-06-2006

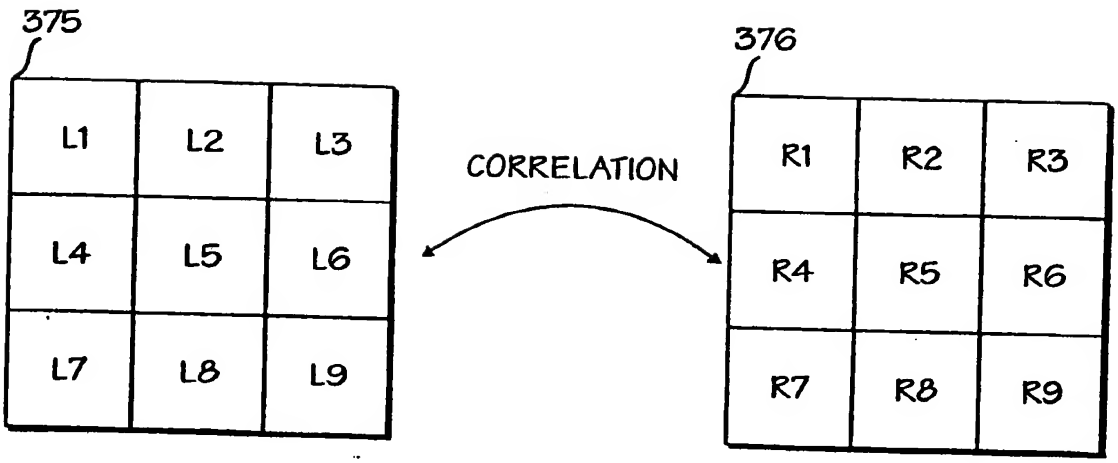


Fig. 12

20120 29802001

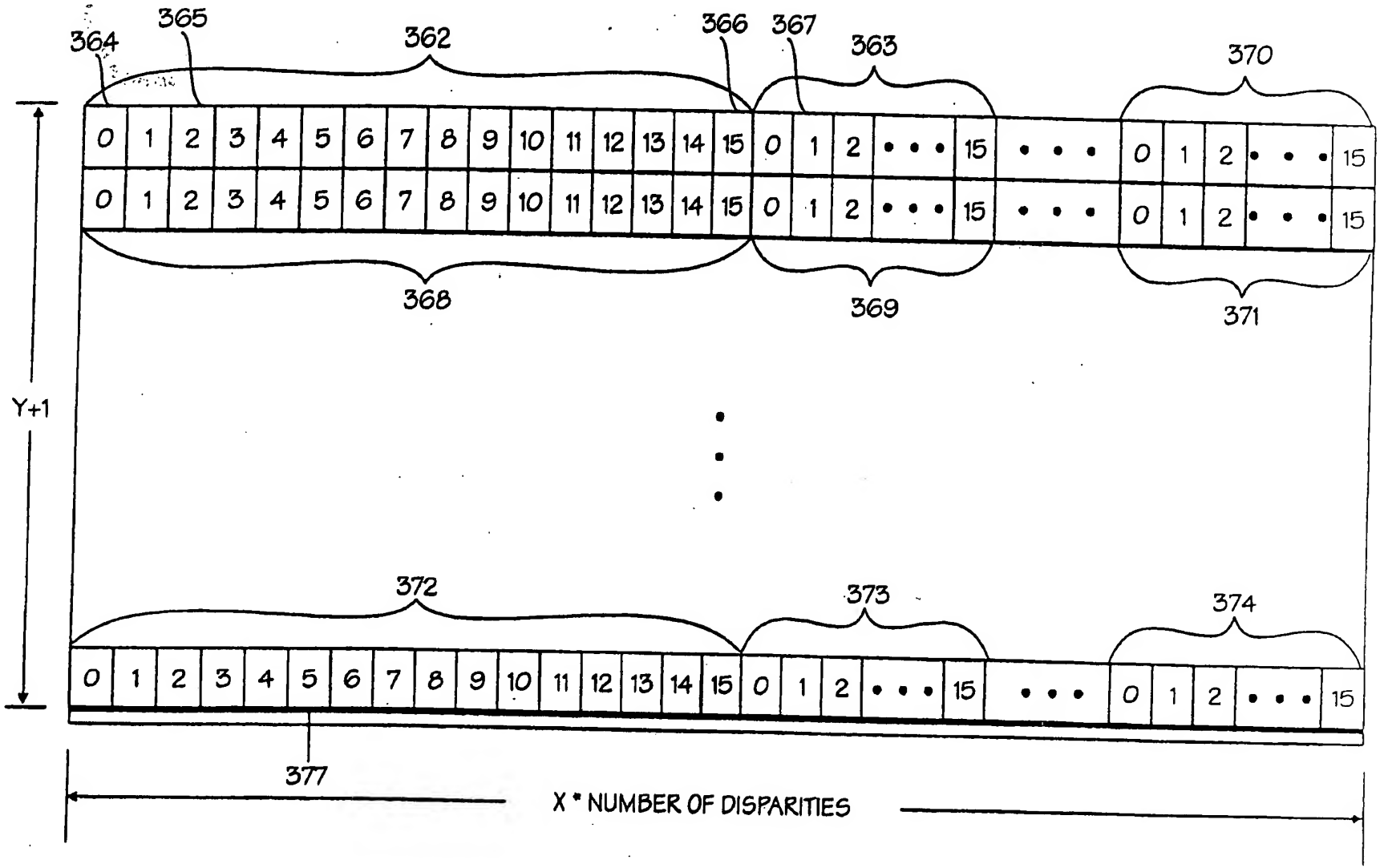
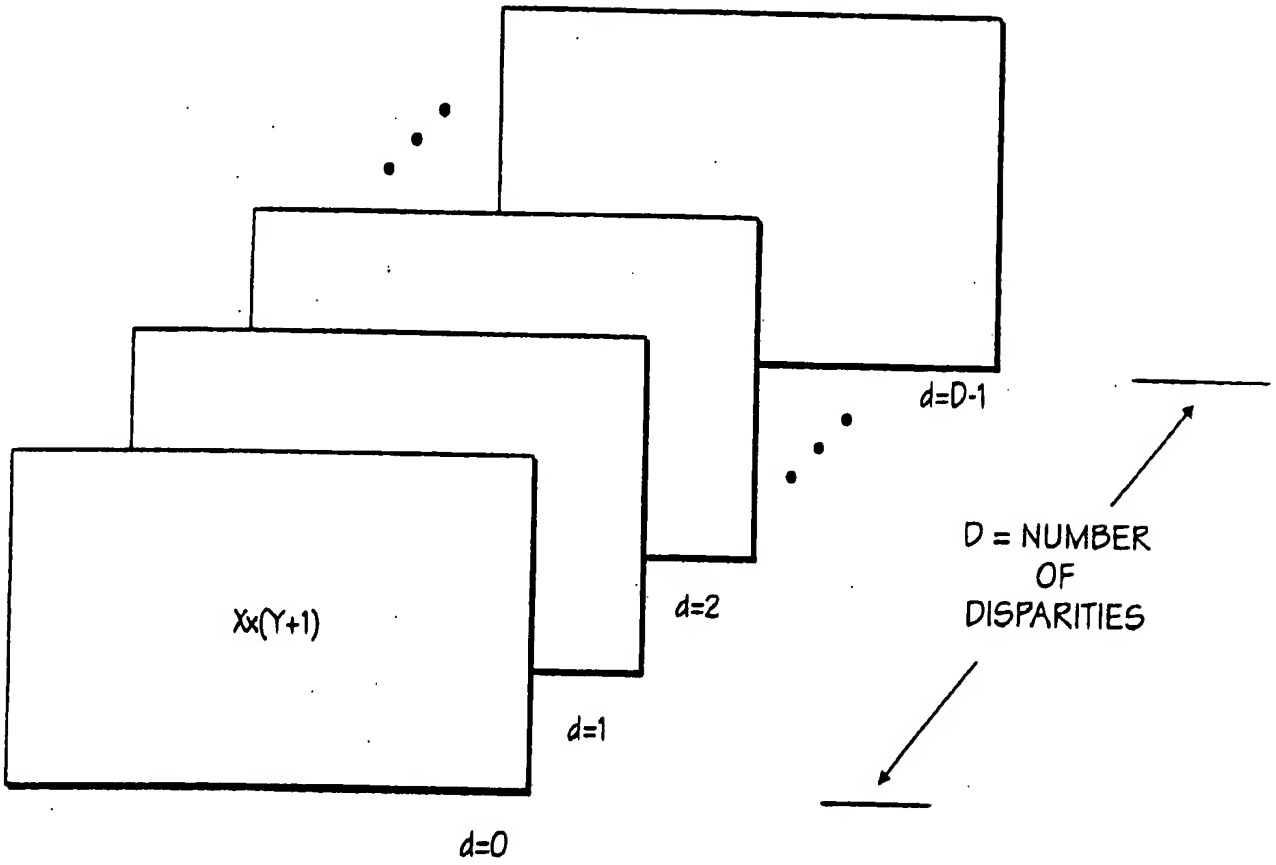


Fig. 13A

20T280 29802001



(B)

Fig. 13B

EP 1 230 639 B1 20060802

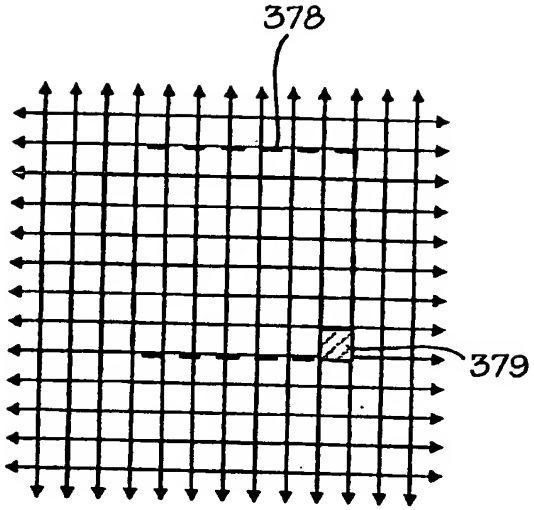


FIG. 14(A)

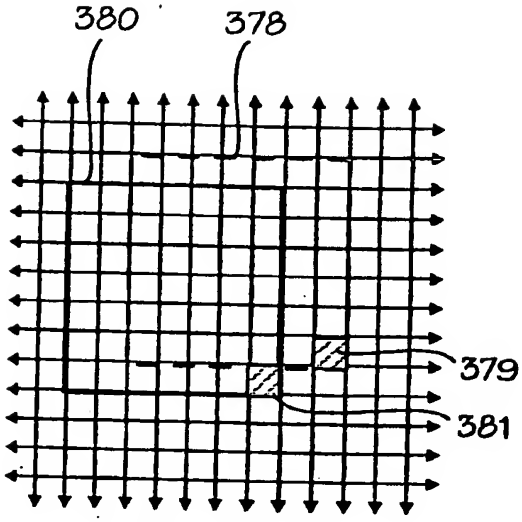


FIG. 14(B)

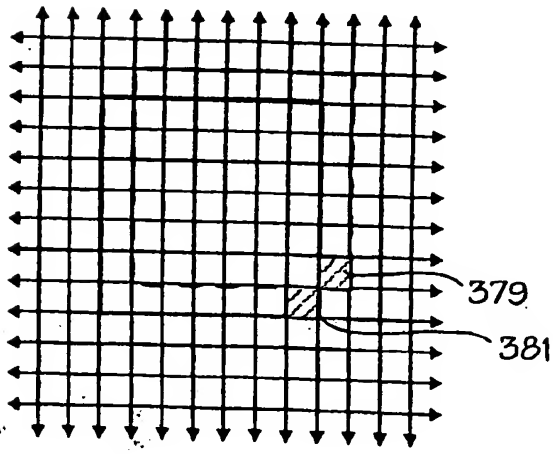


FIG. 14(C)

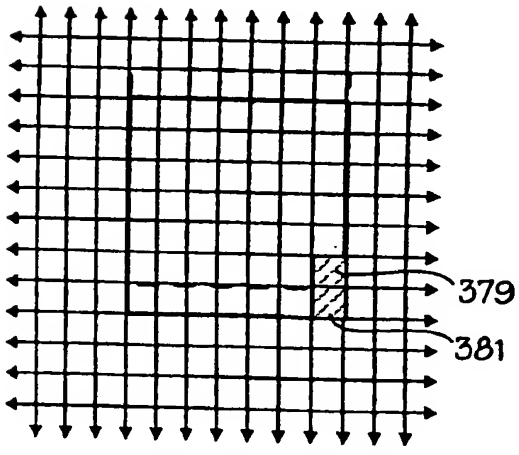


FIG. 14(D)

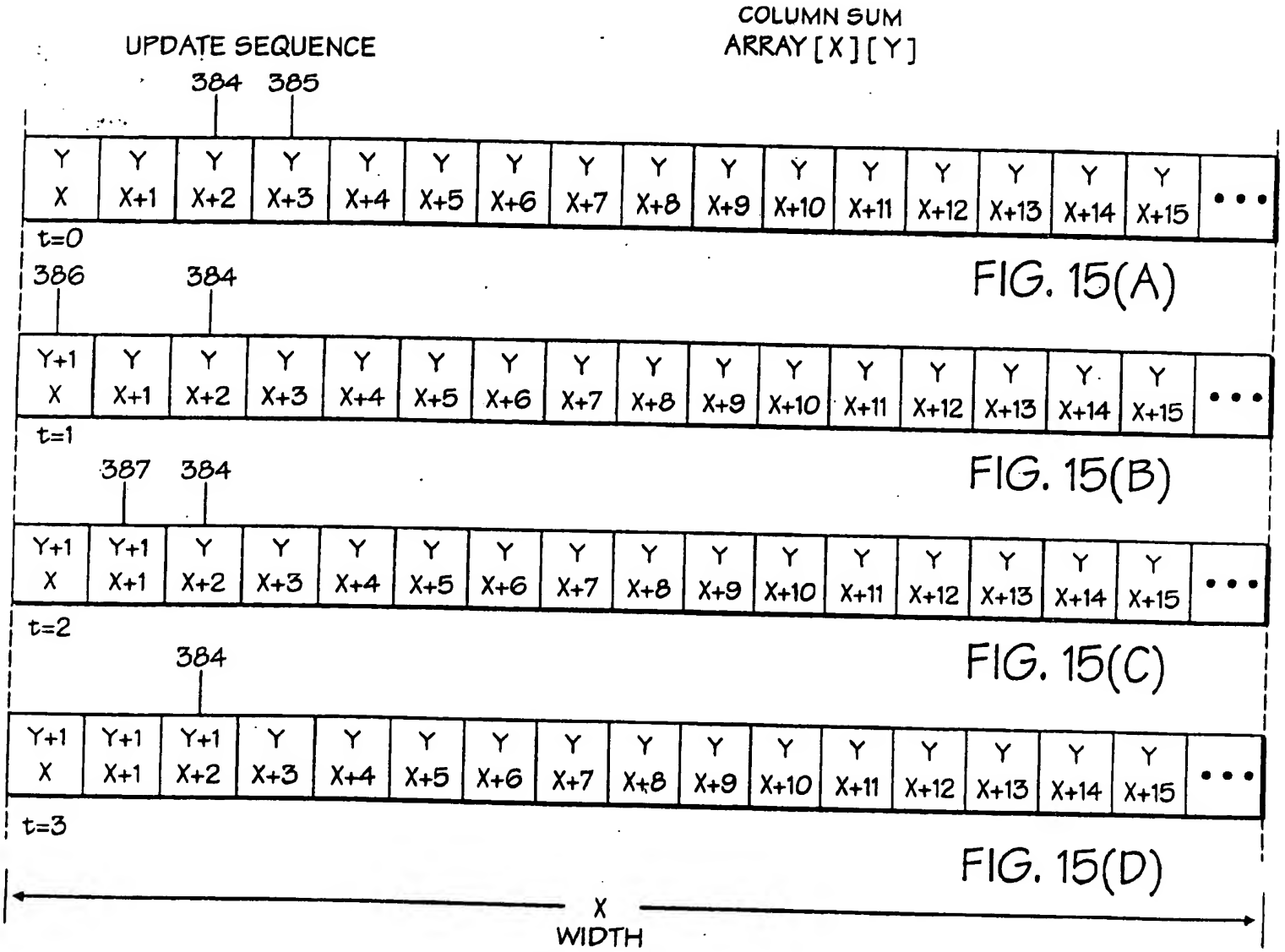


FIG. 15(A)

FIG. 15(B)

FIG. 15(C)

FIG. 15(D)

RIGHT IMAGE = REFERENCE
LEFT IMAGE RIGHT IMAGE

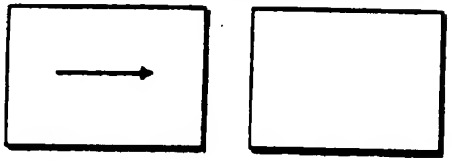


Fig. 16A Fig. 16B

RIGHT IMAGE = REFERENCE
LEFT IMAGE RIGHT IMAGE

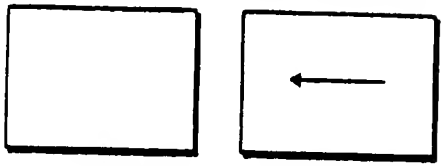


Fig. 16C Fig. 16D

CENSUS VECTORS
LEFT IMAGE

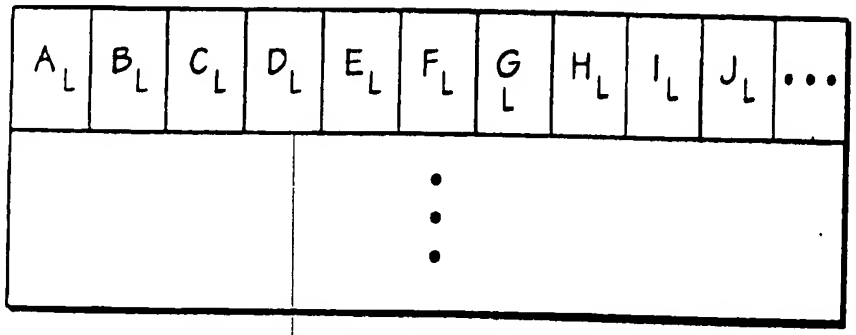


Fig. 16E

CENSUS VECTORS
RIGHT IMAGE

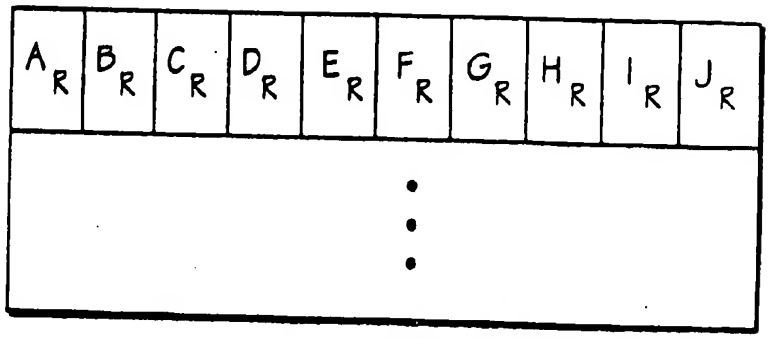
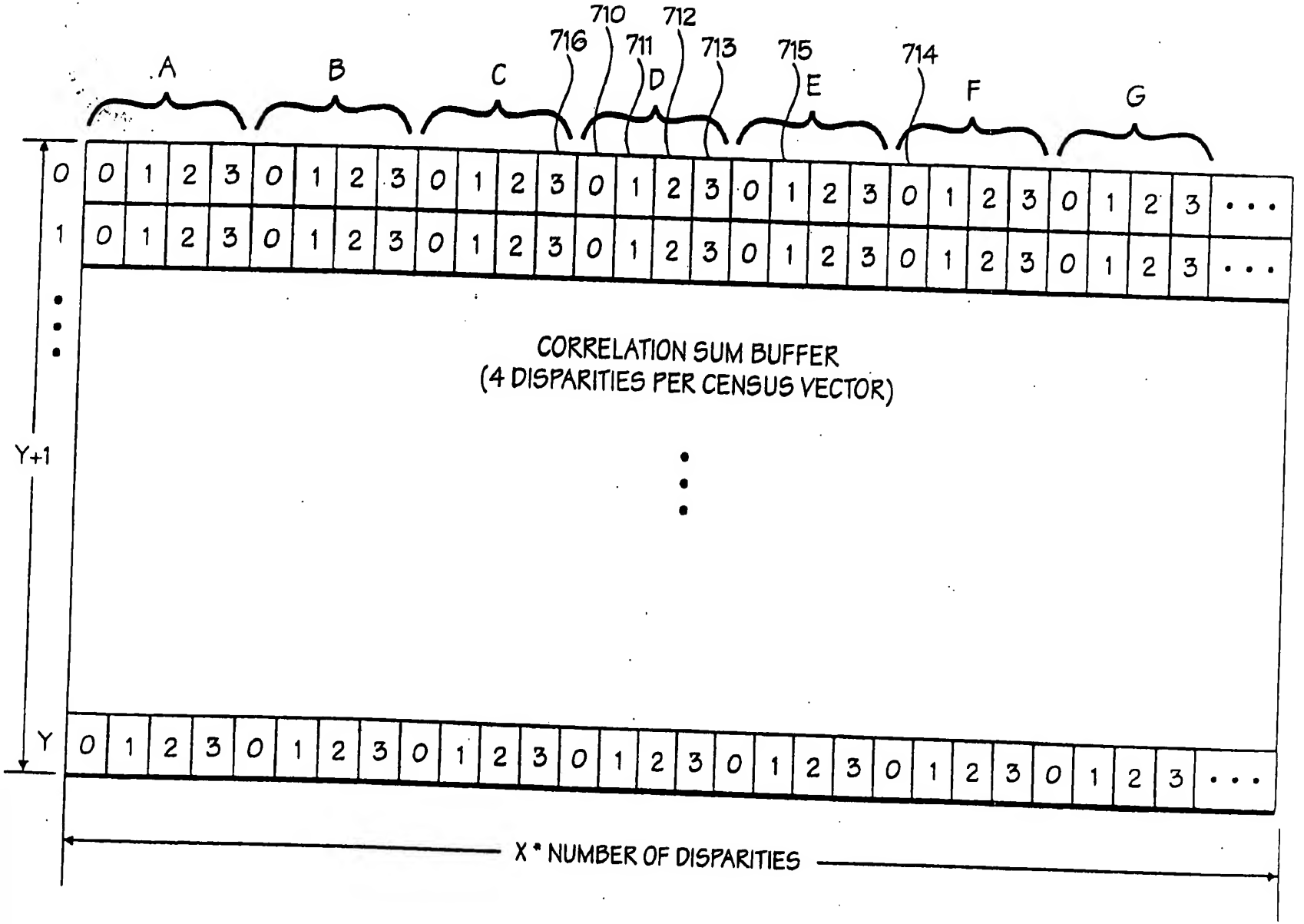


Fig. 16F

20T2EO" 2980200T


A
B
C
716
710
711
712
D
713
715
E
714
F
G
0
1
Y+1
Y
0 1 2 3 0 1 2 3 0 1 2 3

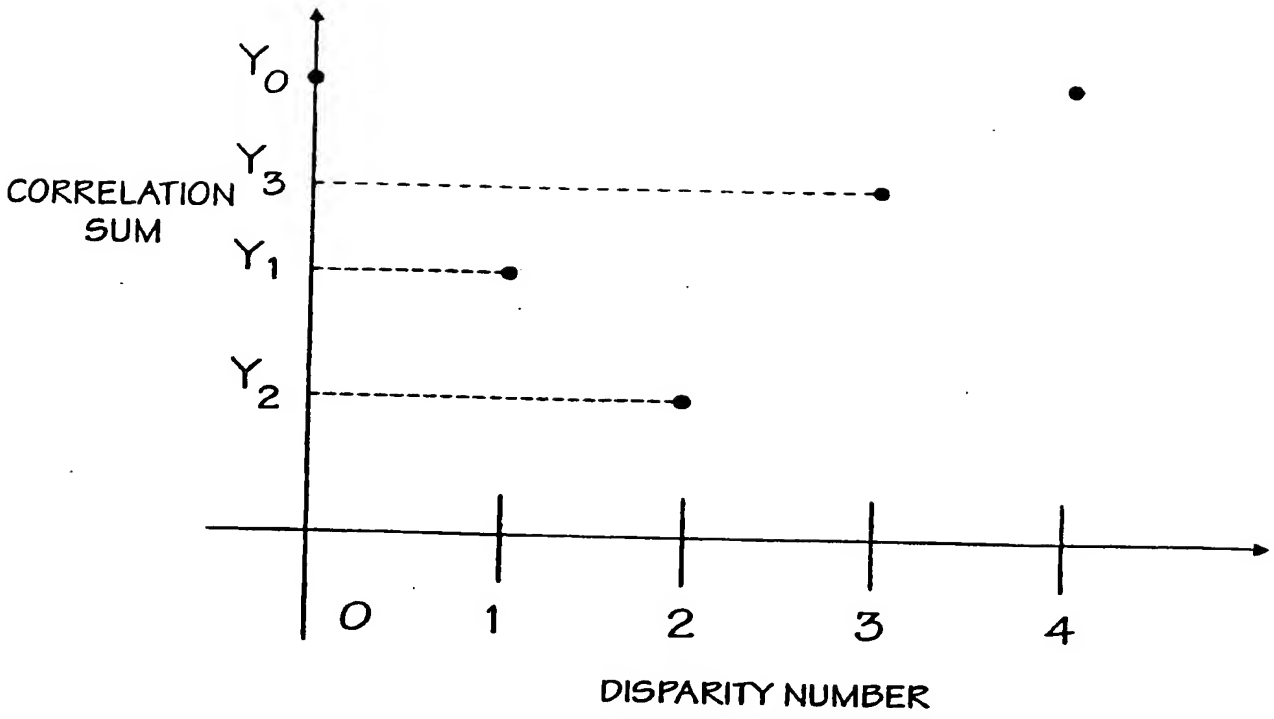


FIG. 17(A)

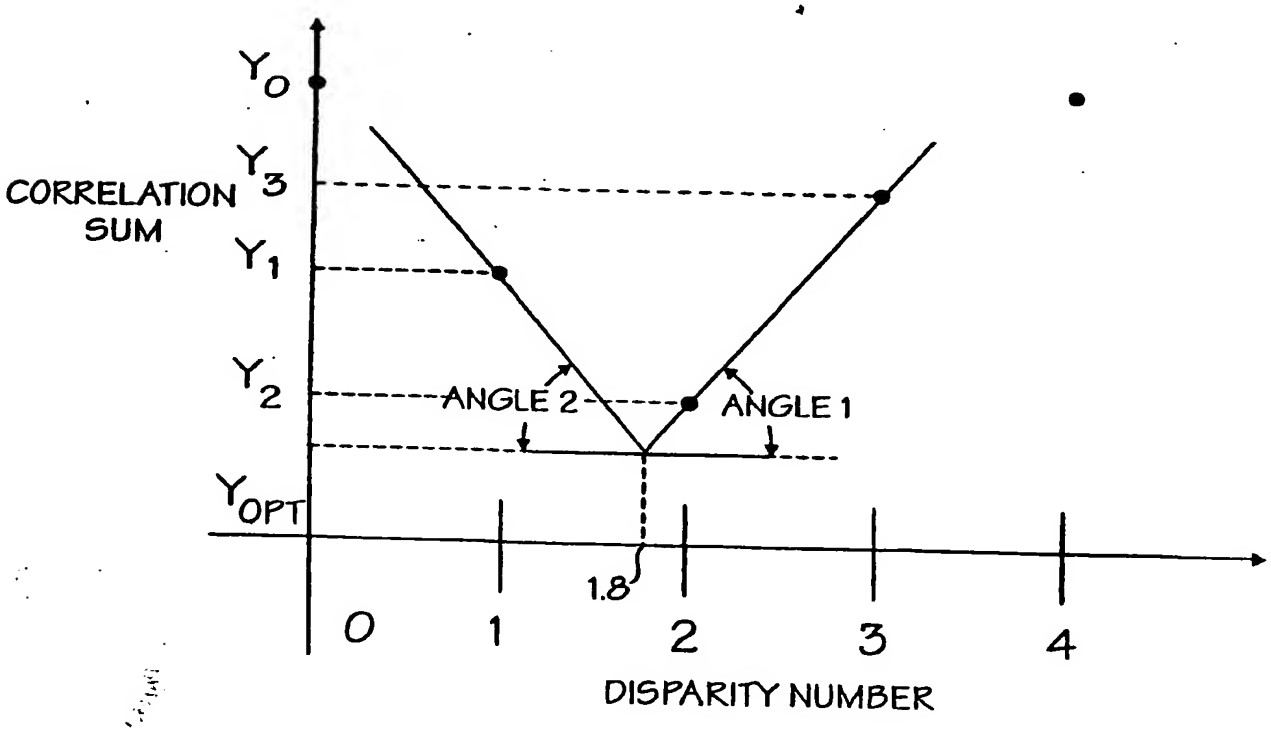


FIG. 17(B)

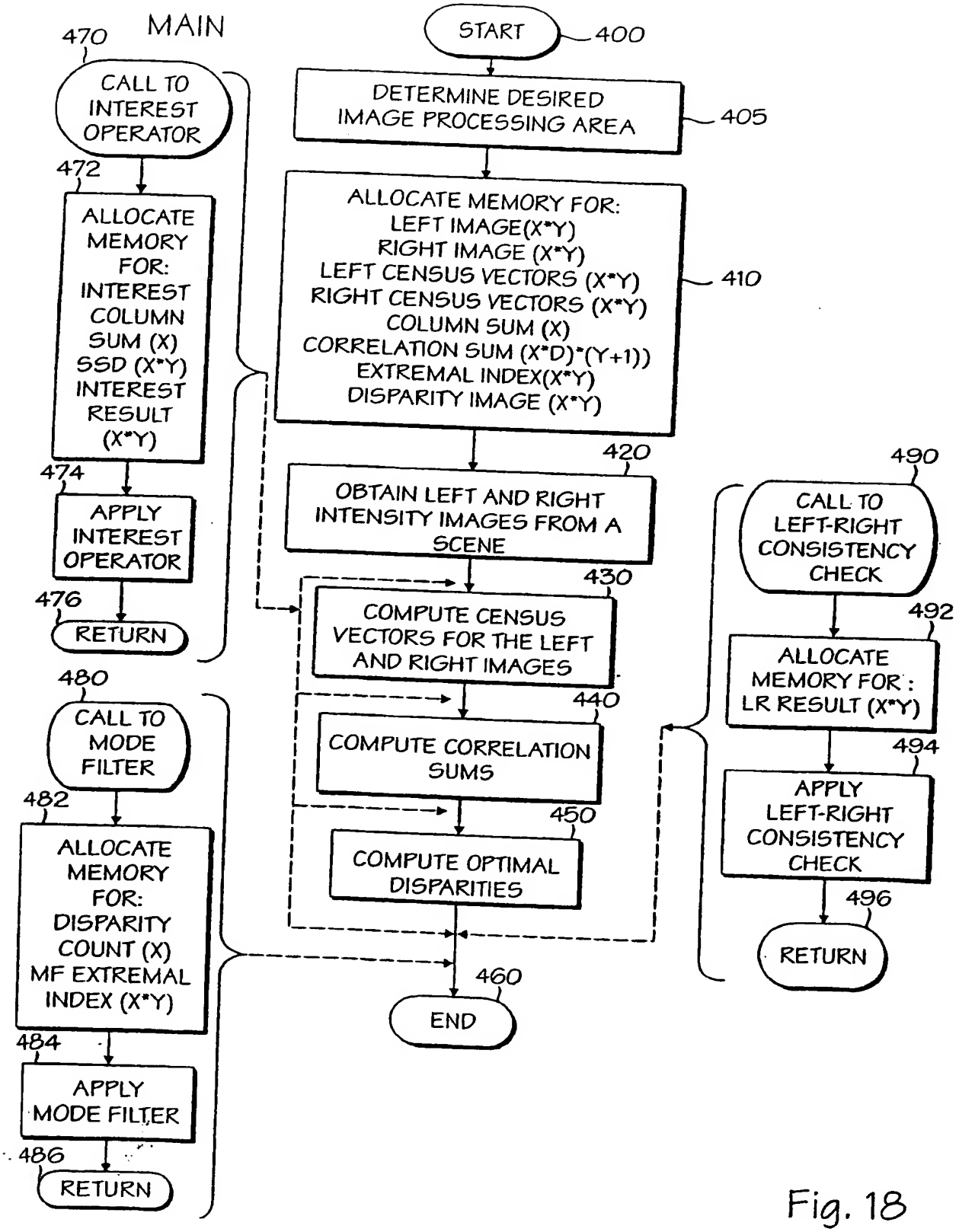

MAIN
START
400
DETERMINE DESIRED IMAGE PROCESSING AREA
405
ALLOCATE MEMORY FOR:
LEFT IMAGE(X*Y)
RIGHT IMAGE (X*Y)
LEFT CENSUS VECTORS (X*Y)
RIGHT CENSUS VECTORS (X*Y)
COLUMN SUM (X)
CORRELATION SUM (X*D)*(Y+1))
EXTREMAL INDEX(X*Y)
DISPARITY IMAGE (X*Y)
410
OBTAIN LEFT AND RIGHT INTENSITY IMAGES FROM A SCENE
420
COMPUTE CENSUS VECTORS FOR THE LEFT AND RIGHT IMAGES
430
COMPUTE CORRELATION SUMS
440
COMPUTE OPTIMAL DISPARITIES
450
END
460
470
CALL TO INTEREST OPERATOR
472
ALLOCATE MEMORY FOR:
INTEREST
COLUMN SUM (X)
SSD (X*Y)
INTEREST RESULT (X*Y)
474
APPLY INTEREST OPERATOR
476
RETURN
480
CALL TO MODE FILTER
482
ALLOCATE MEMORY FOR:
DISPARITY COUNT (X)
MF EXTREMAL INDEX (X*Y)
484
APPLY MODE FILTER
486
RETURN
490
CALL TO LEFT-RIGHT CONSISTENCY CHECK
492
ALLOCATE MEMORY FOR: LR RESULT (X*Y)
494
APPLY LEFT-RIGHT CONSISTENCY CHECK
496
RETURN

Fig. 18

CENSUS TRANSFORM
&
CENSUS VECTORS

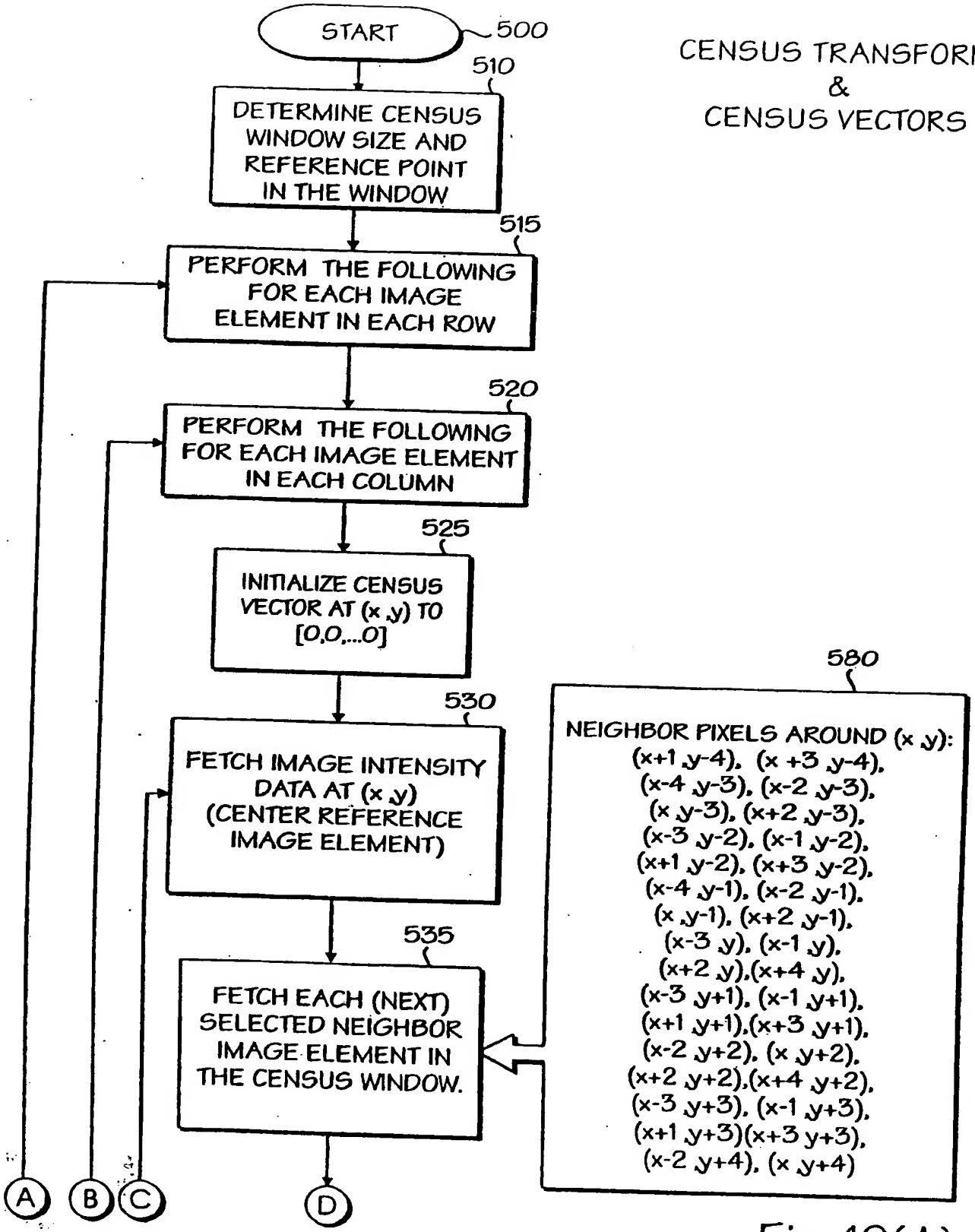


Fig. 19(A)

CENSUS TRANSFORM
&
CENSUS VECTORS

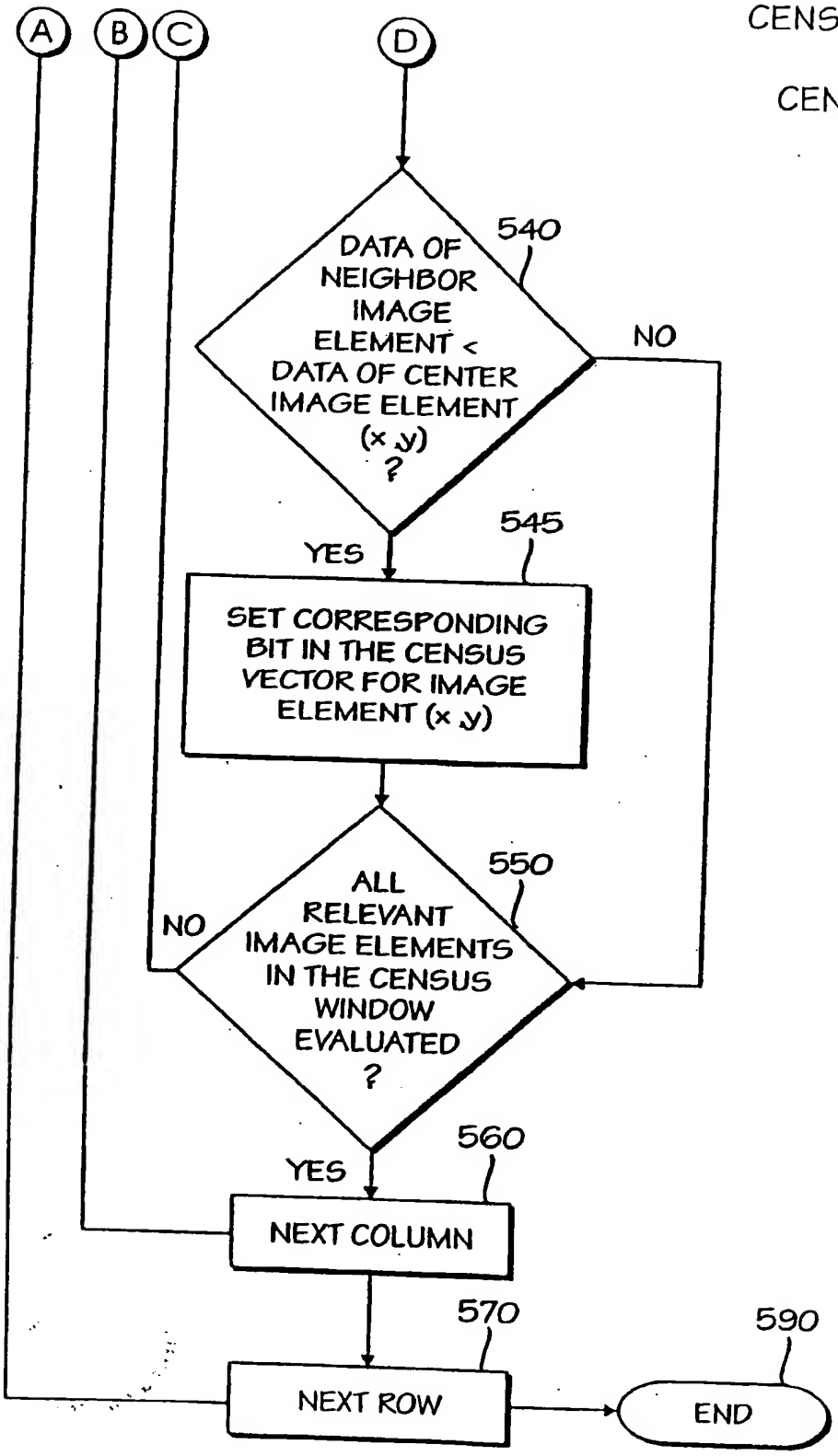


Fig. 19(B)

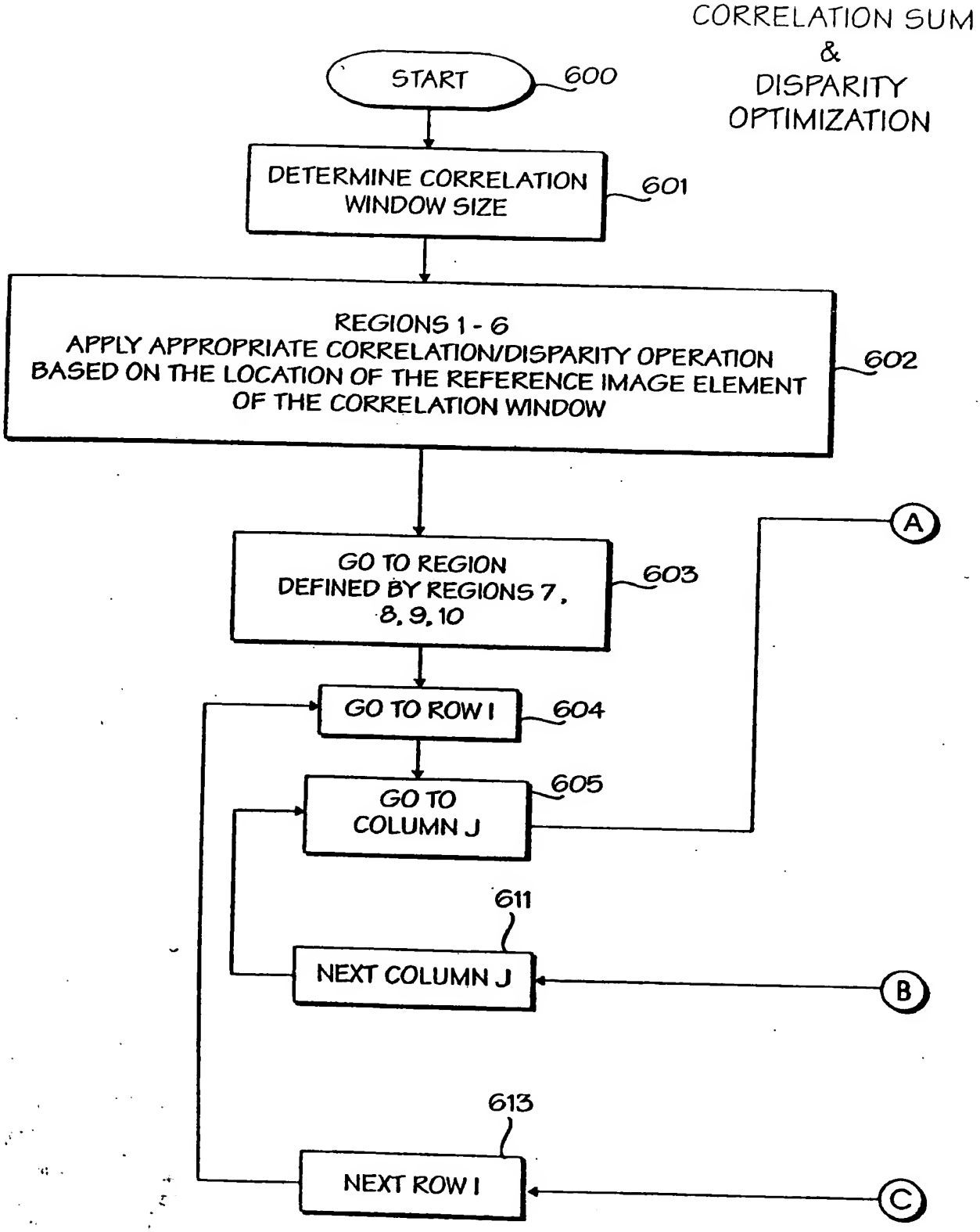

CORRELATION SUM
&
DISPARITY
OPTIMIZATION
START
600
DETERMINE CORRELATION WINDOW SIZE
601
REGIONS 1 - 6
APPLY APPROPRIATE CORRELATION/DISPARITY OPERATION BASED ON THE LOCATION OF THE REFERENCE IMAGE ELEMENT OF THE CORRELATION WINDOW
602
GO TO REGION DEFINED BY REGIONS 7, 8, 9, 10
603
A
GO TO ROW I
604
GO TO COLUMN J
605
611
NEXT COLUMN J
B
613
NEXT ROW I
C

Fig. 20(A)

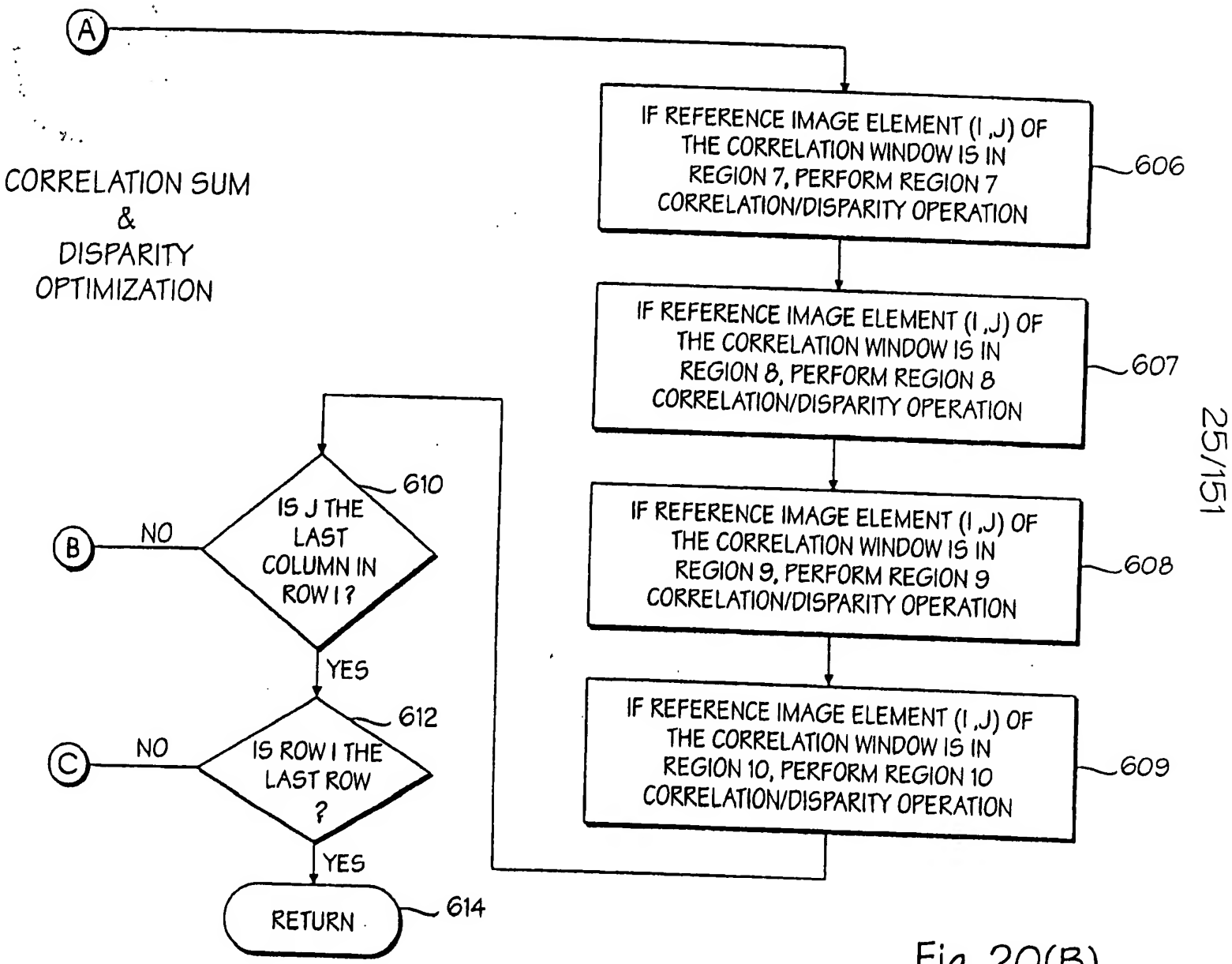

A
CORRELATION SUM & DISPARITY OPTIMIZATION
IF REFERENCE IMAGE ELEMENT (I ,J) OF THE CORRELATION WINDOW IS IN REGION 7, PERFORM REGION 7 CORRELATION/DISPARITY OPERATION
606
IF REFERENCE IMAGE ELEMENT (I ,J) OF THE CORRELATION WINDOW IS IN REGION 8, PERFORM REGION 8 CORRELATION/DISPARITY OPERATION
607
IF REFERENCE IMAGE ELEMENT (I ,J) OF THE CORRELATION WINDOW IS IN REGION 9, PERFORM REGION 9 CORRELATION/DISPARITY OPERATION
608
IF REFERENCE IMAGE ELEMENT (I ,J) OF THE CORRELATION WINDOW IS IN REGION 10, PERFORM REGION 10 CORRELATION/DISPARITY OPERATION
609
610
IS J THE LAST COLUMN IN ROW I ?
B
NO
YES
612
IS ROW I THE LAST ROW ?
C
NO
YES
RETURN
614

Fig. 20(B)

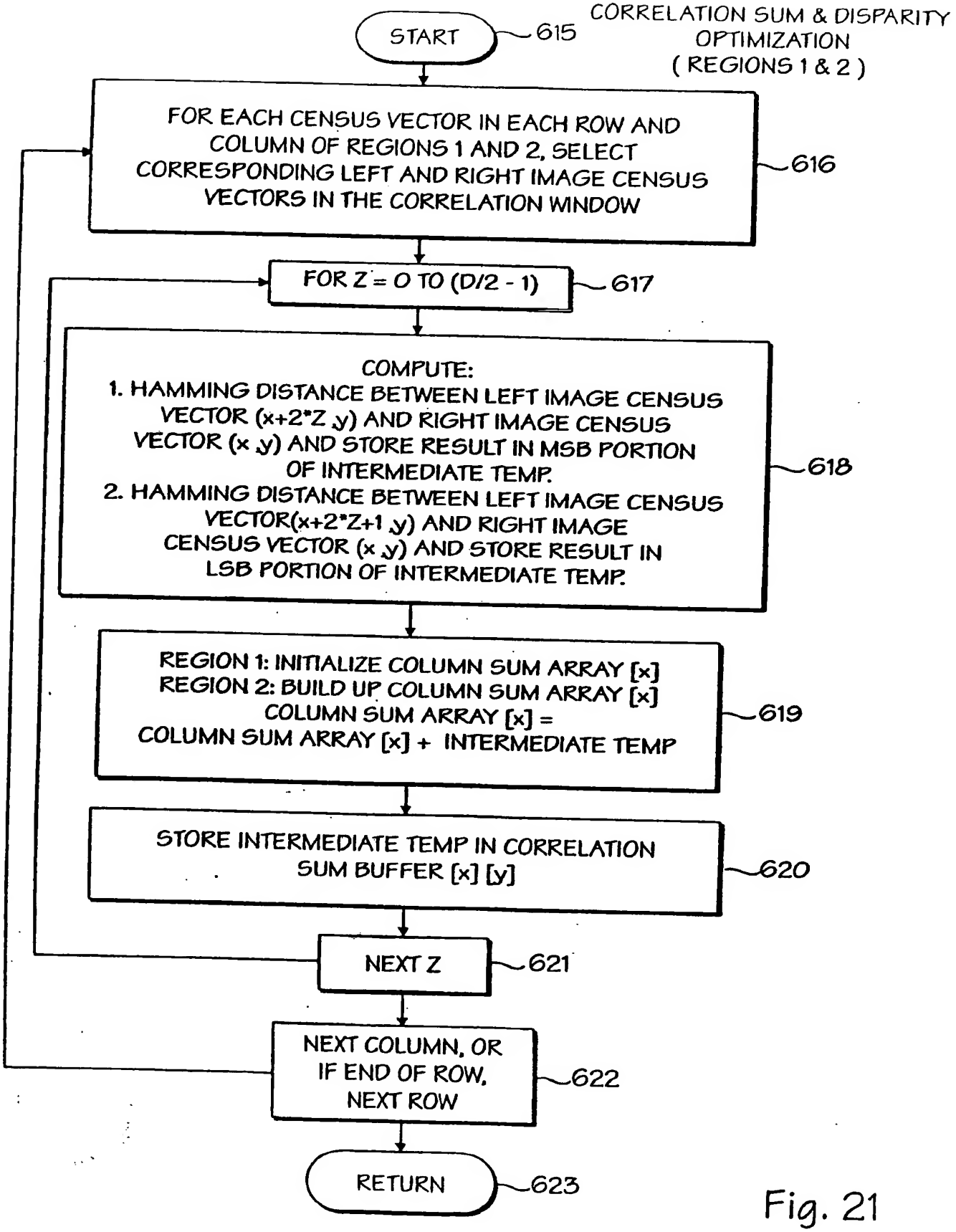

CORRELATION SUM & DISPARITY OPTIMIZATION (REGIONS 1 & 2)
START
615
FOR EACH CENSUS VECTOR IN EACH ROW AND COLUMN OF REGIONS 1 AND 2, SELECT CORRESPONDING LEFT AND RIGHT IMAGE CENSUS VECTORS IN THE CORRELATION WINDOW
616
FOR Z = 0 TO (D/2 - 1)
617
COMPUTE:
1. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*Z ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN MSB PORTION OF INTERMEDIATE TEMP.
2. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR(x+2*Z+1 ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN LSB PORTION OF INTERMEDIATE TEMP.
618
REGION 1: INITIALIZE COLUMN SUM ARRAY [x]
REGION 2: BUILD UP COLUMN SUM ARRAY [x]
COLUMN SUM ARRAY [x] =
COLUMN SUM ARRAY [x] + INTERMEDIATE TEMP
619
STORE INTERMEDIATE TEMP IN CORRELATION SUM BUFFER [x] [y]
620
NEXT Z
621
NEXT COLUMN, OR IF END OF ROW, NEXT ROW
622
RETURN
623

Fig. 21

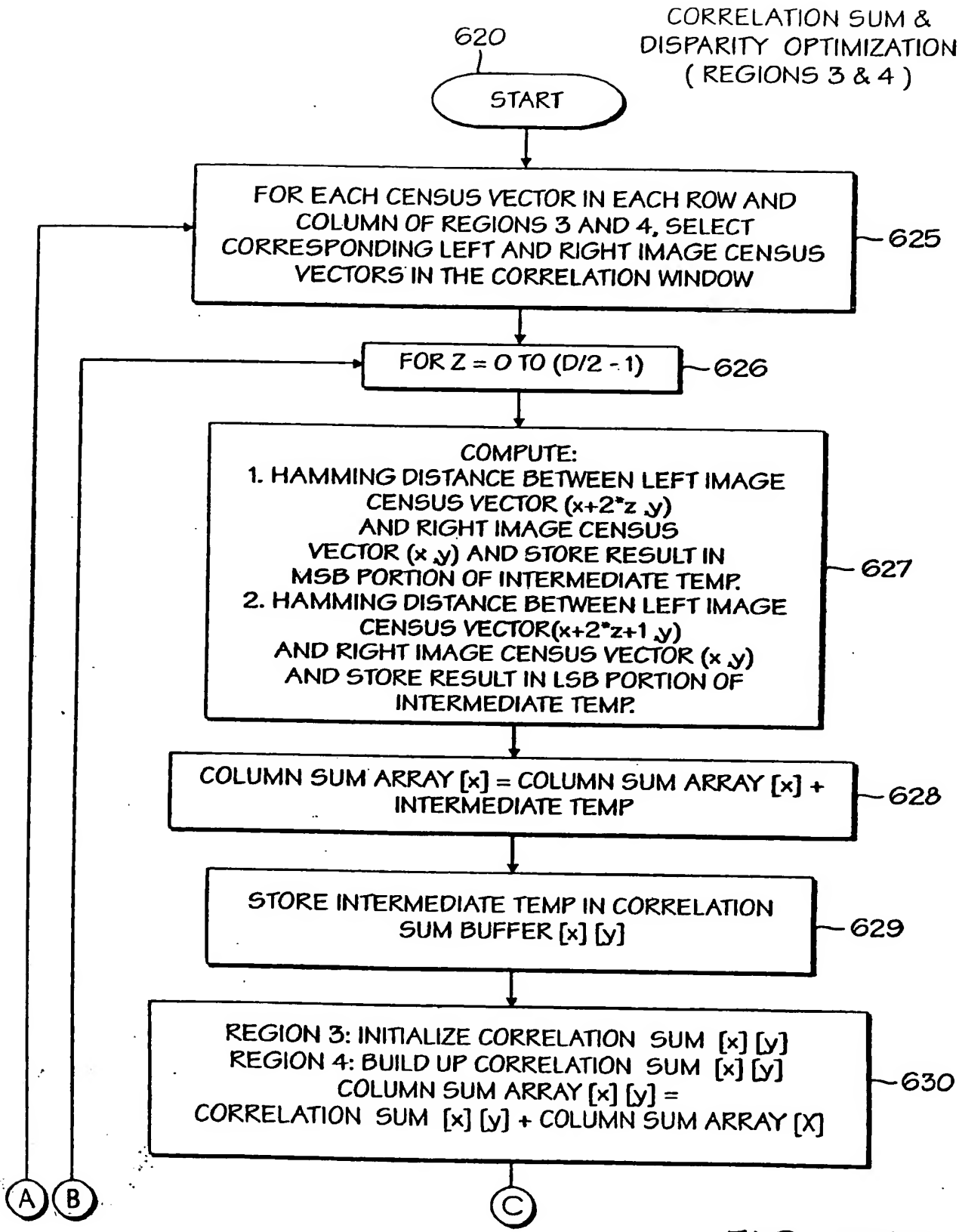

CORRELATION SUM &
DISPARITY OPTIMIZATION
(REGIONS 3 & 4)
620
START
FOR EACH CENSUS VECTOR IN EACH ROW AND COLUMN OF REGIONS 3 AND 4, SELECT CORRESPONDING LEFT AND RIGHT IMAGE CENSUS VECTORS IN THE CORRELATION WINDOW
625
FOR Z = 0 TO (D/2 - 1)
626
COMPUTE:
1. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN MSB PORTION OF INTERMEDIATE TEMP.
2. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR(x+2*z+1 ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN LSB PORTION OF INTERMEDIATE TEMP.
627
COLUMN SUM ARRAY [x] = COLUMN SUM ARRAY [x] + INTERMEDIATE TEMP
628
STORE INTERMEDIATE TEMP IN CORRELATION SUM BUFFER [x] [y]
629
REGION 3: INITIALIZE CORRELATION SUM [x] [y]
REGION 4: BUILD UP CORRELATION SUM [x] [y]
COLUMN SUM ARRAY [x] [y] =
CORRELATION SUM [x] [y] + COLUMN SUM ARRAY [X]
630
A
B
C

FIG. 22(A)

CORRELATION SUM &
DISPARITY OPTIMIZATION
(REGIONS 3 & 4)

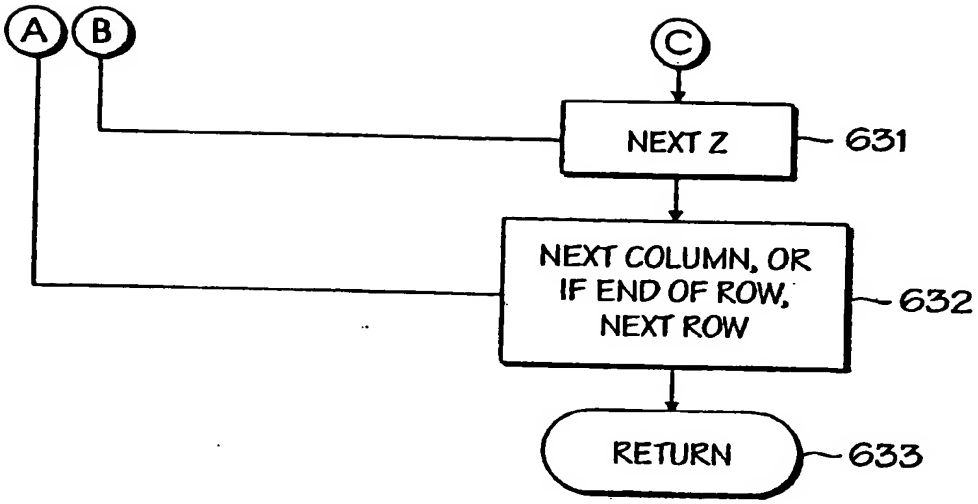


FIG. 22(B)

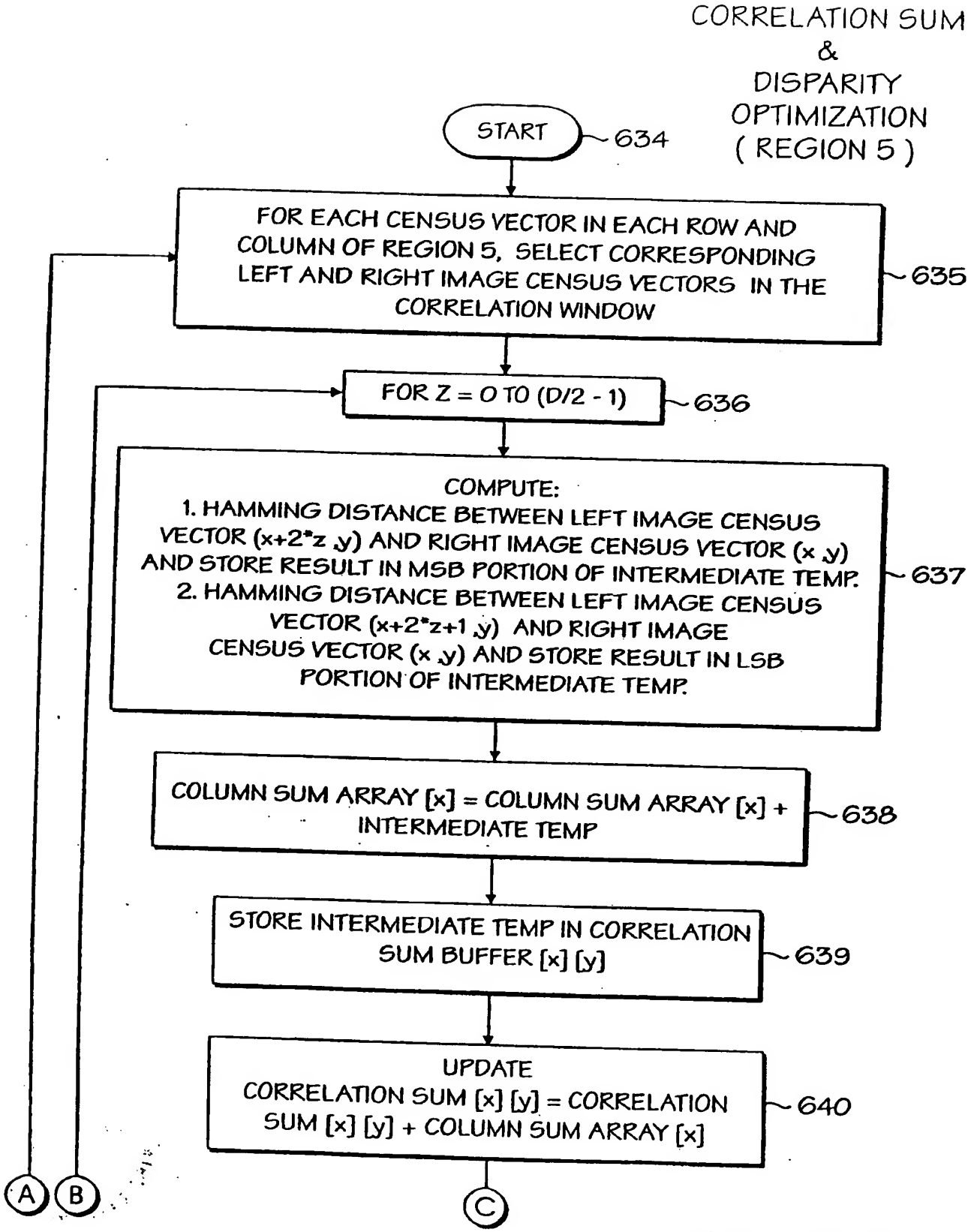
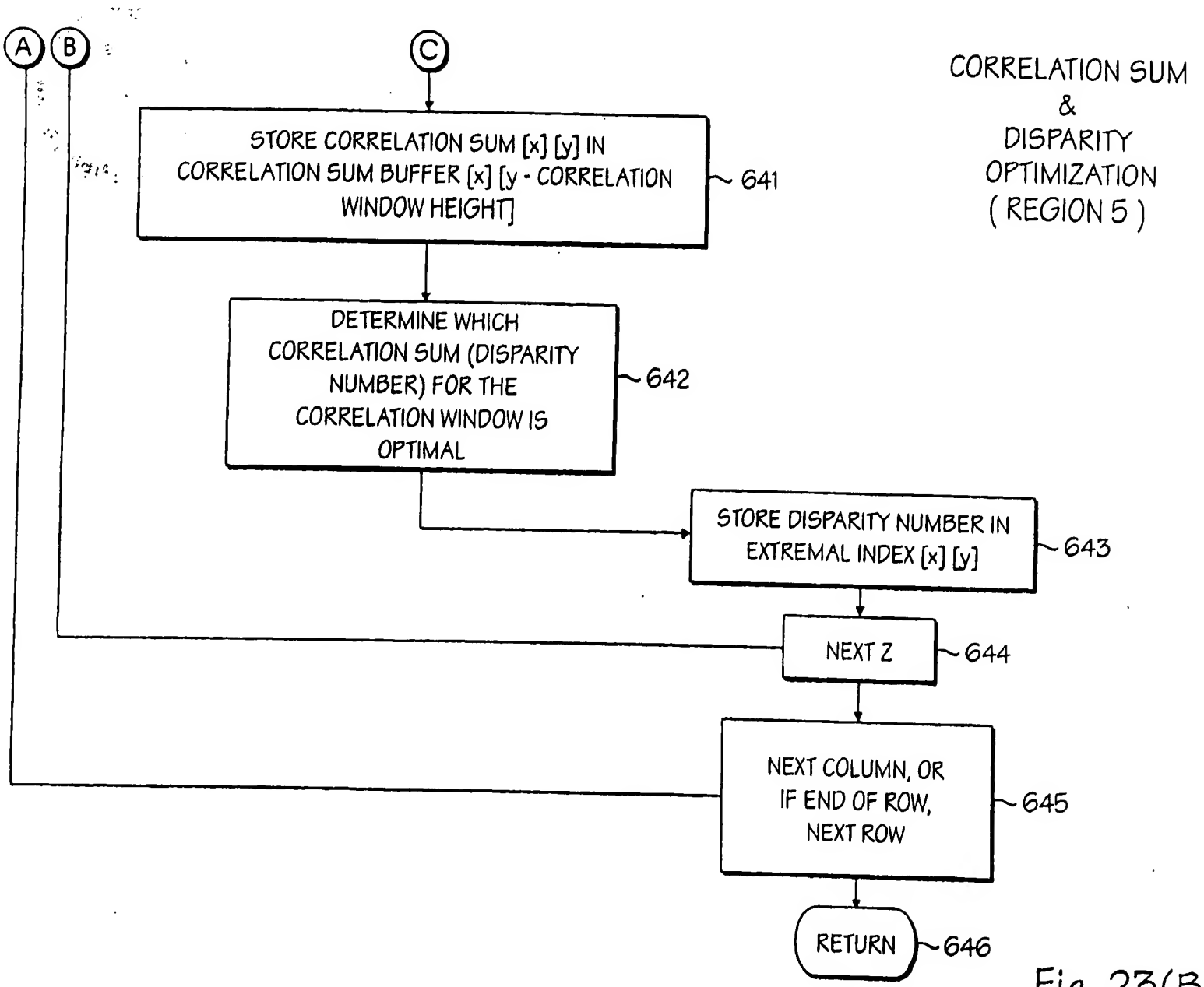

CORRELATION SUM
&
DISPARITY
OPTIMIZATION
(REGION 5)
START
634
FOR EACH CENSUS VECTOR IN EACH ROW AND COLUMN OF REGION 5, SELECT CORRESPONDING LEFT AND RIGHT IMAGE CENSUS VECTORS IN THE CORRELATION WINDOW
635
FOR Z = 0 TO (D/2 - 1)
636
COMPUTE:
1. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN MSB PORTION OF INTERMEDIATE TEMP.
2. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z+1 ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN LSB PORTION OF INTERMEDIATE TEMP.
637
COLUMN SUM ARRAY [x] = COLUMN SUM ARRAY [x] + INTERMEDIATE TEMP
638
STORE INTERMEDIATE TEMP IN CORRELATION SUM BUFFER [x] [y]
639
UPDATE
CORRELATION SUM [x] [y] = CORRELATION SUM [x] [y] + COLUMN SUM ARRAY [x]
640
A
B
C

FIG. 23(A)



CORRELATION SUM
&
DISPARITY
OPTIMIZATION
(REGION 5)

Fig. 23(B)

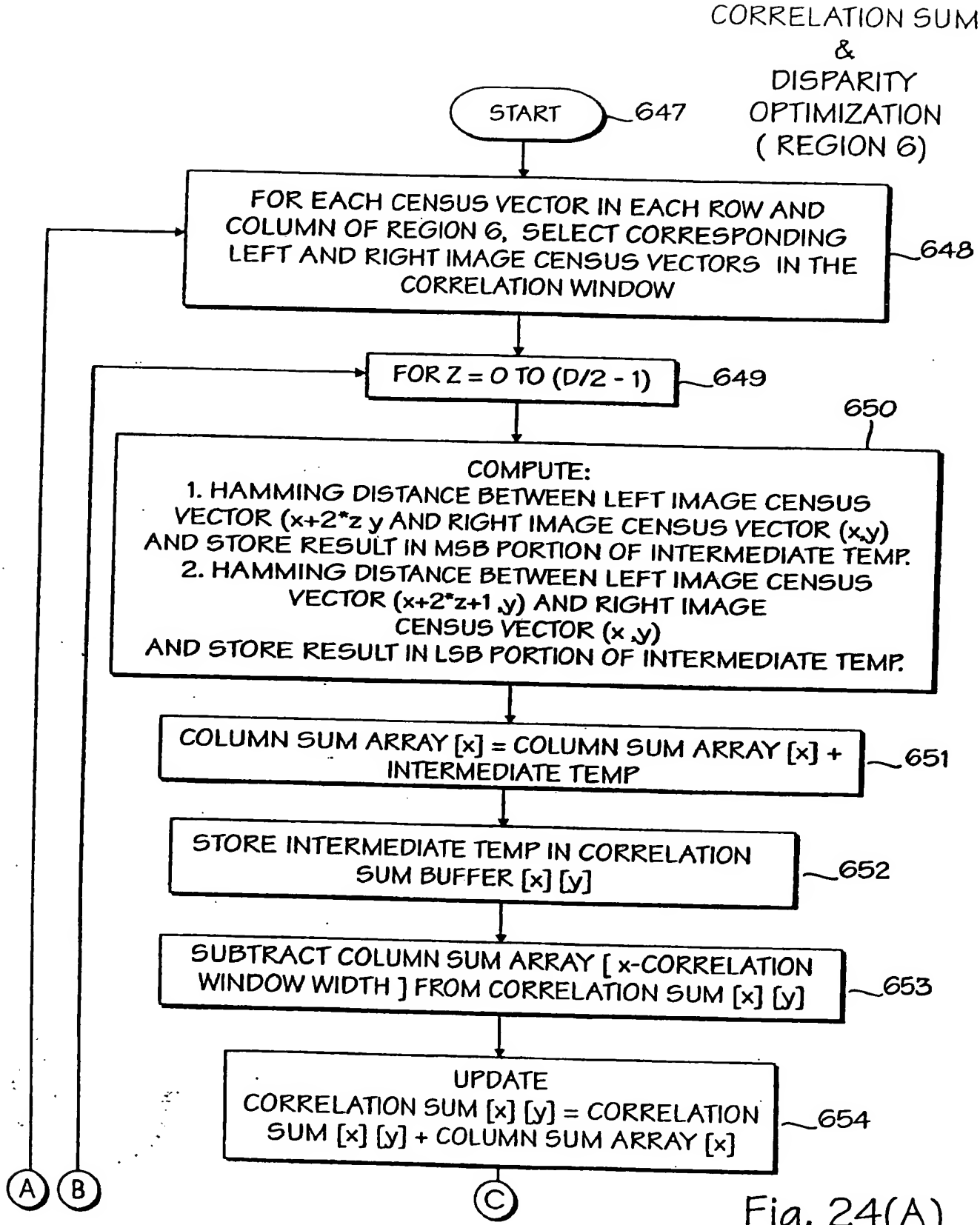

CORRELATION SUM
&
DISPARITY
OPTIMIZATION
(REGION 6)
START
647
FOR EACH CENSUS VECTOR IN EACH ROW AND COLUMN OF REGION 6, SELECT CORRESPONDING LEFT AND RIGHT IMAGE CENSUS VECTORS IN THE CORRELATION WINDOW
648
FOR Z = 0 TO (D/2 - 1)
649
650
COMPUTE:
1. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z y AND RIGHT IMAGE CENSUS VECTOR (x,y) AND STORE RESULT IN MSB PORTION OF INTERMEDIATE TEMP.
2. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z+1 ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y)
AND STORE RESULT IN LSB PORTION OF INTERMEDIATE TEMP.
COLUMN SUM ARRAY [x] = COLUMN SUM ARRAY [x] + INTERMEDIATE TEMP
651
STORE INTERMEDIATE TEMP IN CORRELATION SUM BUFFER [x] [y]
652
SUBTRACT COLUMN SUM ARRAY [x-CORRELATION WINDOW WIDTH] FROM CORRELATION SUM [x] [y]
653
UPDATE
CORRELATION SUM [x] [y] = CORRELATION SUM [x] [y] + COLUMN SUM ARRAY [x]
654
A
B
C

Fig. 24(A)

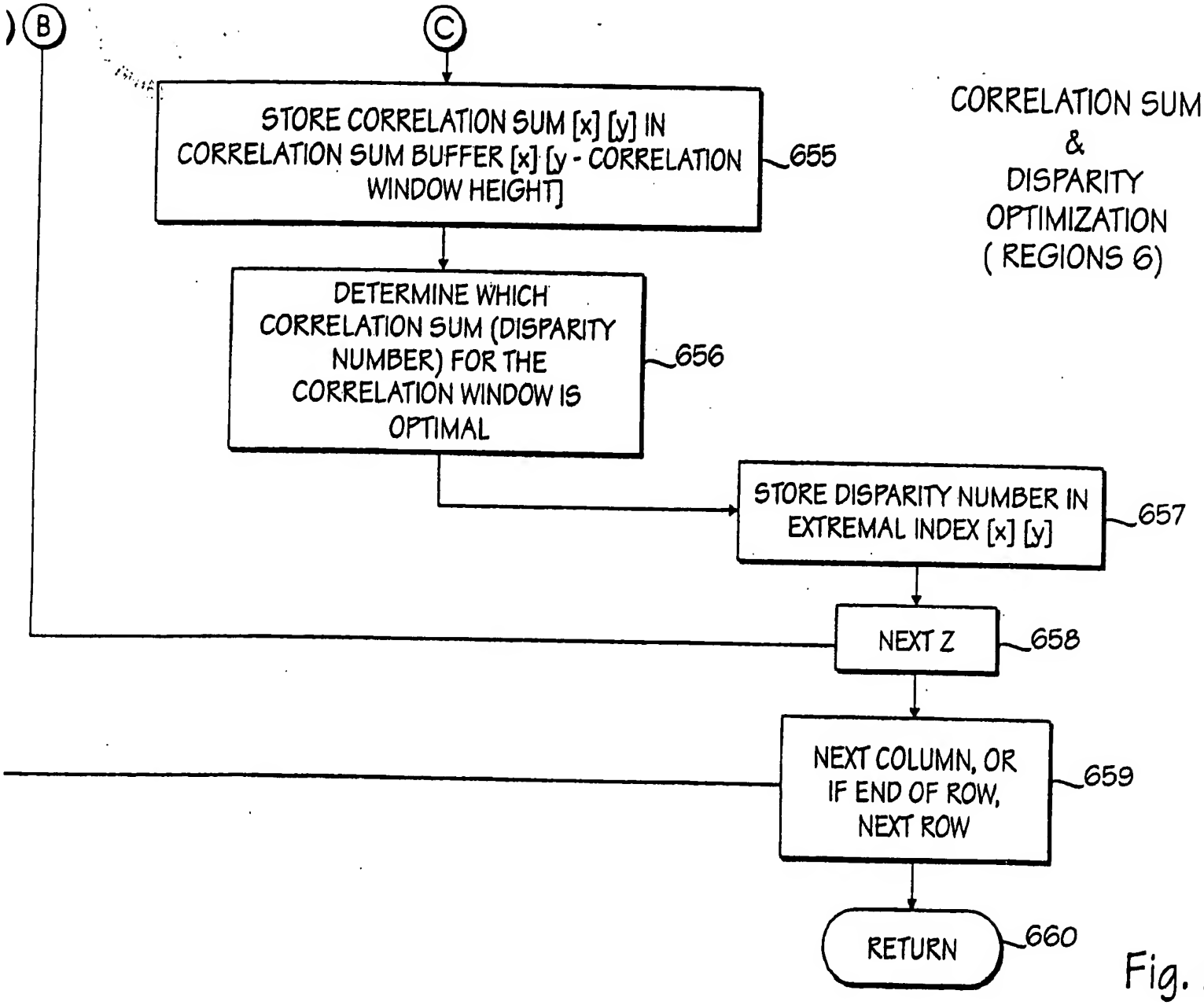

B
C
STORE CORRELATION SUM [x] [y] IN CORRELATION SUM BUFFER [x] [y - CORRELATION WINDOW HEIGHT]
655
DETERMINE WHICH CORRELATION SUM (DISPARITY NUMBER) FOR THE CORRELATION WINDOW IS OPTIMAL
656
STORE DISPARITY NUMBER IN EXTREMAL INDEX [x] [y]
657
NEXT Z
658
NEXT COLUMN, OR IF END OF ROW, NEXT ROW
659
RETURN
660
CORRELATION SUM & DISPARITY OPTIMIZATION (REGIONS 6)

Fig. 24(B)

CORRELATION SUM
&
DISPARITY
OPTIMIZATION
(REGIONS 7 & 8)

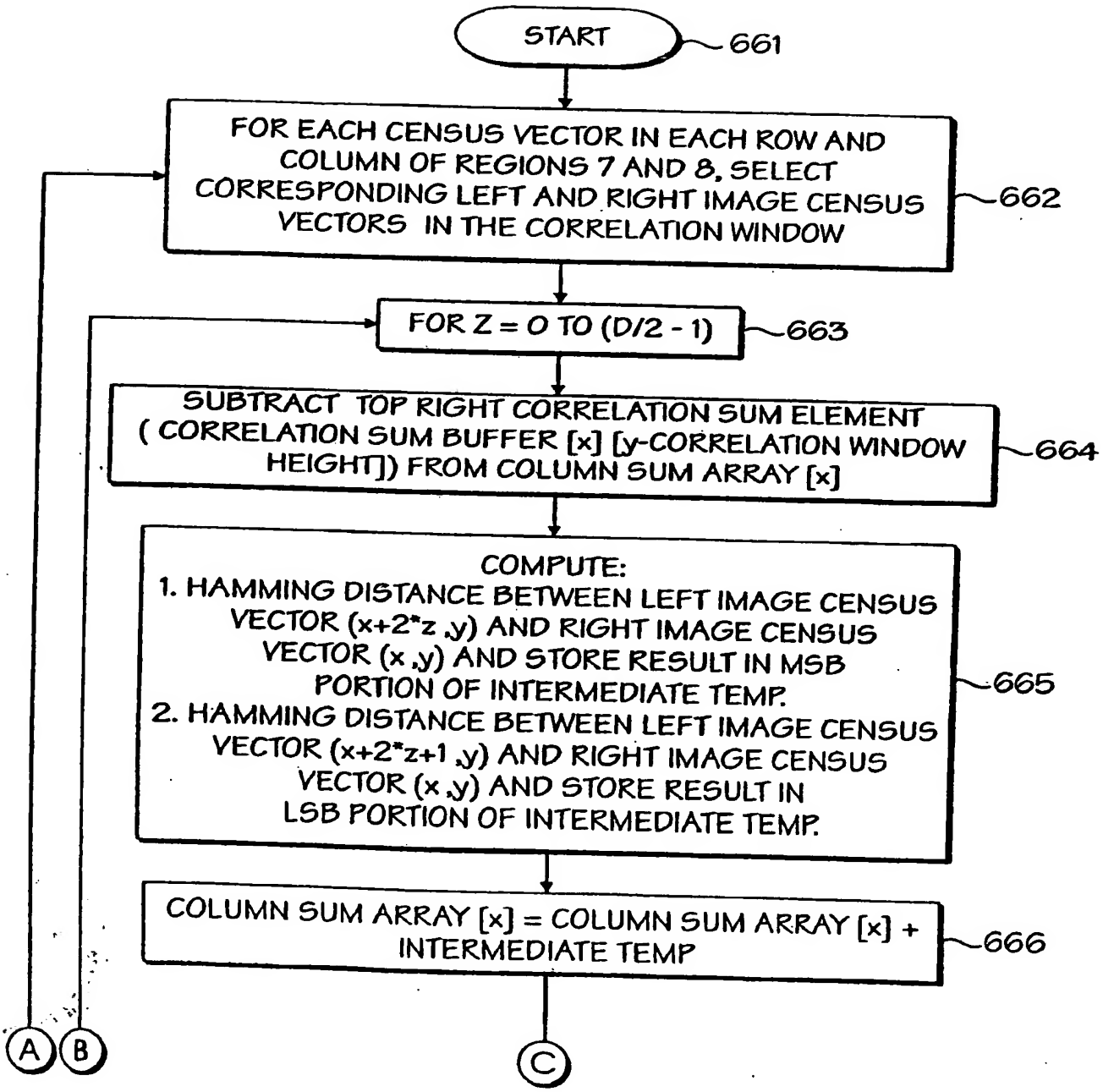


Fig. 25(A)

CORRELATION SUM
&
DISPARITY
OPTIMIZATION
(REGIONS 7 & 8)

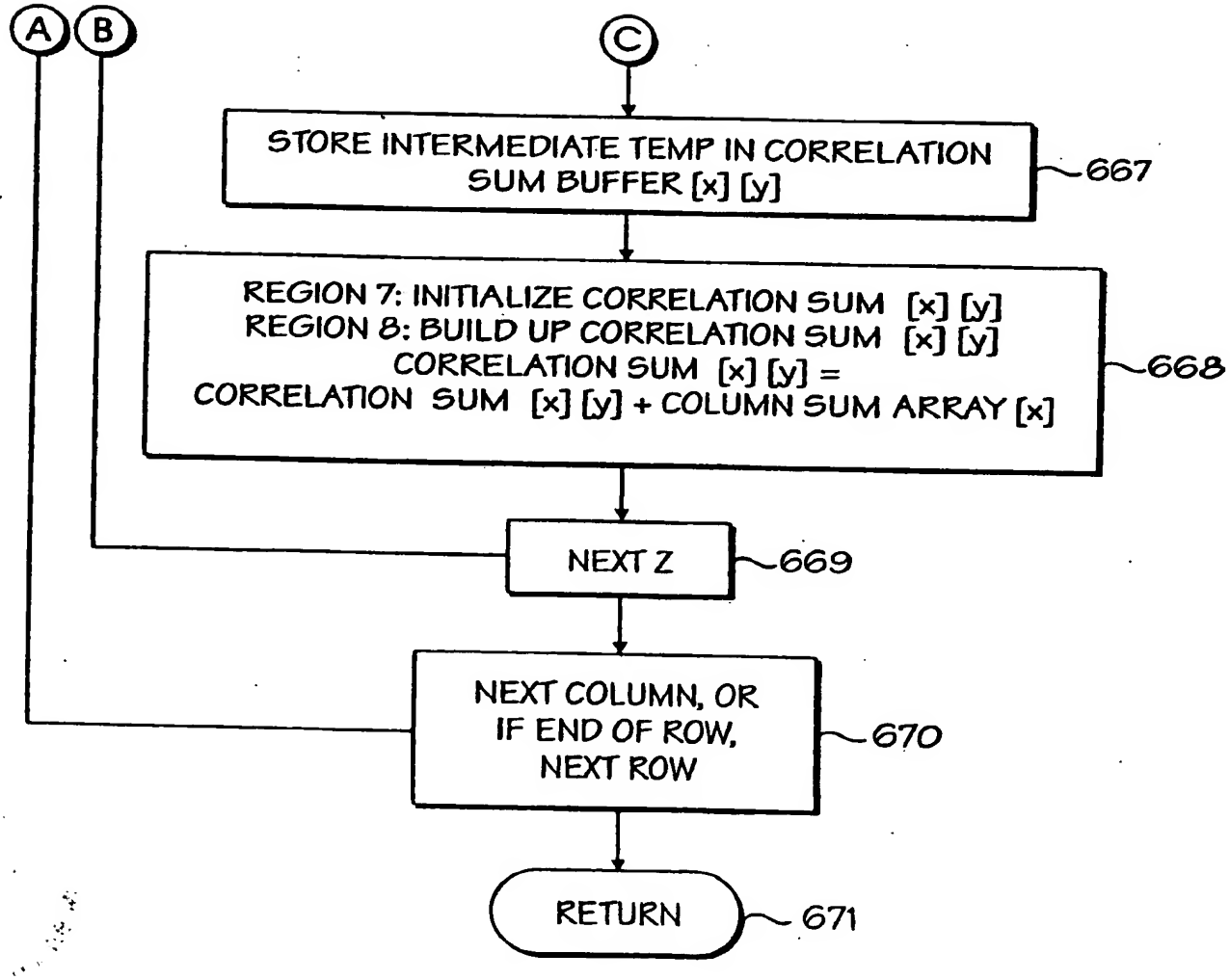


Fig 25(B)

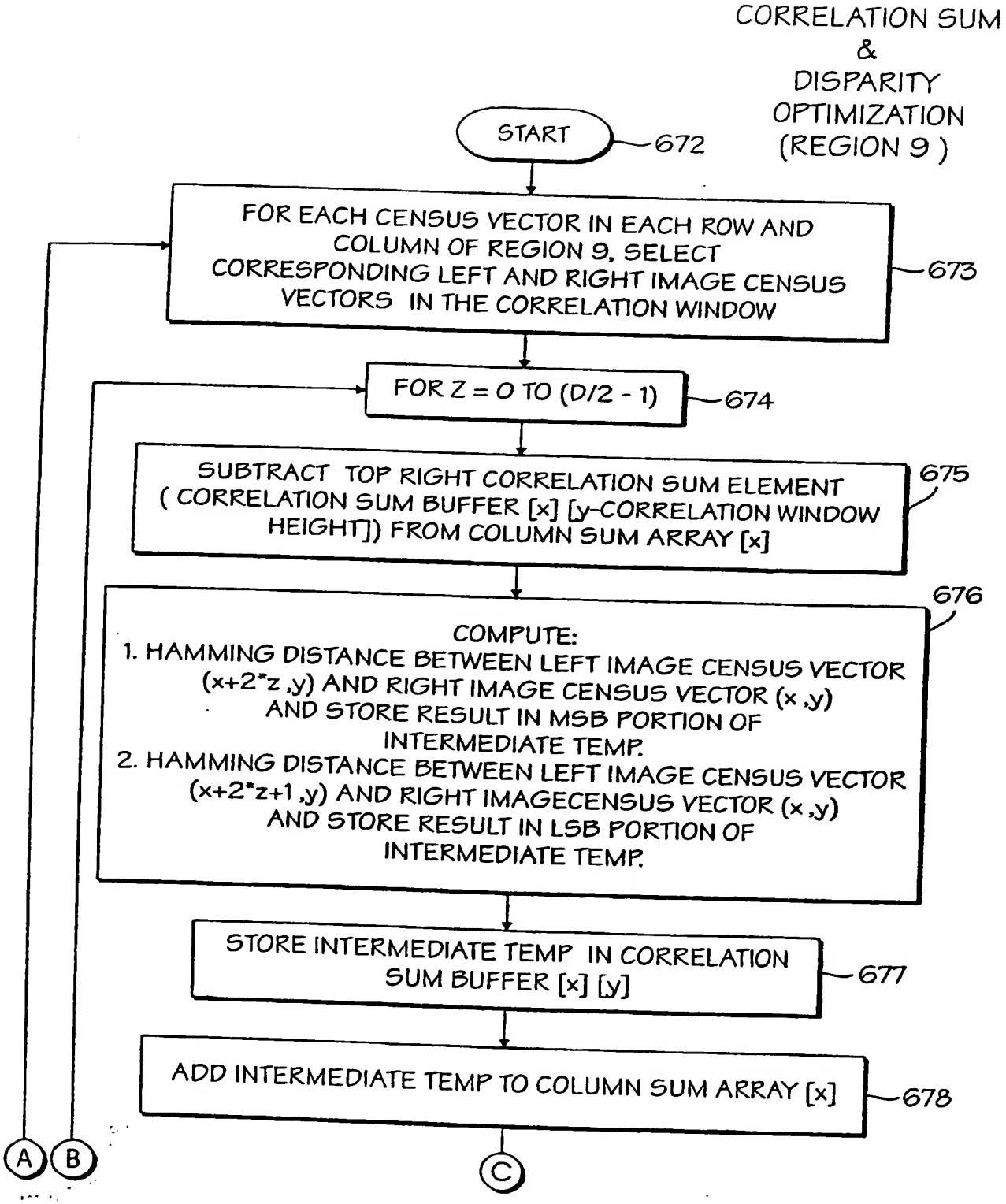

CORRELATION SUM
&
DISPARITY
OPTIMIZATION
(REGION 9)
START
672
FOR EACH CENSUS VECTOR IN EACH ROW AND COLUMN OF REGION 9, SELECT CORRESPONDING LEFT AND RIGHT IMAGE CENSUS VECTORS IN THE CORRELATION WINDOW
673
FOR Z = 0 TO (D/2 - 1)
674
SUBTRACT TOP RIGHT CORRELATION SUM ELEMENT (CORRELATION SUM BUFFER [x] [y-CORRELATION WINDOW HEIGHT]) FROM COLUMN SUM ARRAY [x]
675
676
COMPUTE:
1. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN MSB PORTION OF INTERMEDIATE TEMP.
2. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z+1 ,y) AND RIGHT IMAGECENSUS VECTOR (x ,y) AND STORE RESULT IN LSB PORTION OF INTERMEDIATE TEMP.
STORE INTERMEDIATE TEMP IN CORRELATION SUM BUFFER [x] [y]
677
ADD INTERMEDIATE TEMP TO COLUMN SUM ARRAY [x]
678
A
B
C

FIG. 26(A)

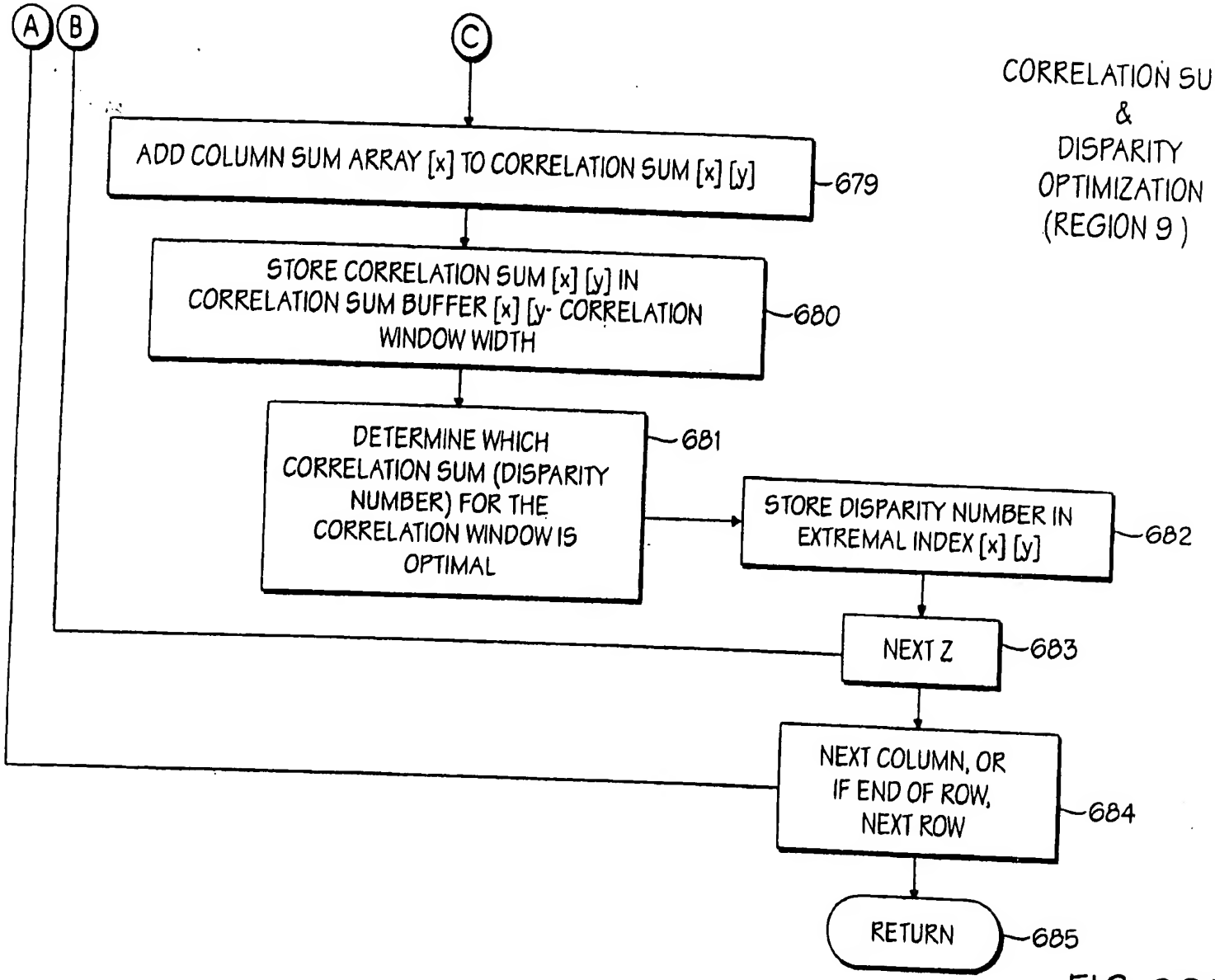

A
B
C
CORRELATION SUM & DISPARITY OPTIMIZATION (REGION 9)
ADD COLUMN SUM ARRAY [x] TO CORRELATION SUM [x] [y]
679
STORE CORRELATION SUM [x] [y] IN CORRELATION SUM BUFFER [x] [y- CORRELATION WINDOW WIDTH
680
DETERMINE WHICH CORRELATION SUM (DISPARITY NUMBER) FOR THE CORRELATION WINDOW IS OPTIMAL
681
STORE DISPARITY NUMBER IN EXTREMAL INDEX [x] [y]
682
NEXT Z
683
NEXT COLUMN, OR IF END OF ROW, NEXT ROW
684
RETURN
685

FIG. 26(B)

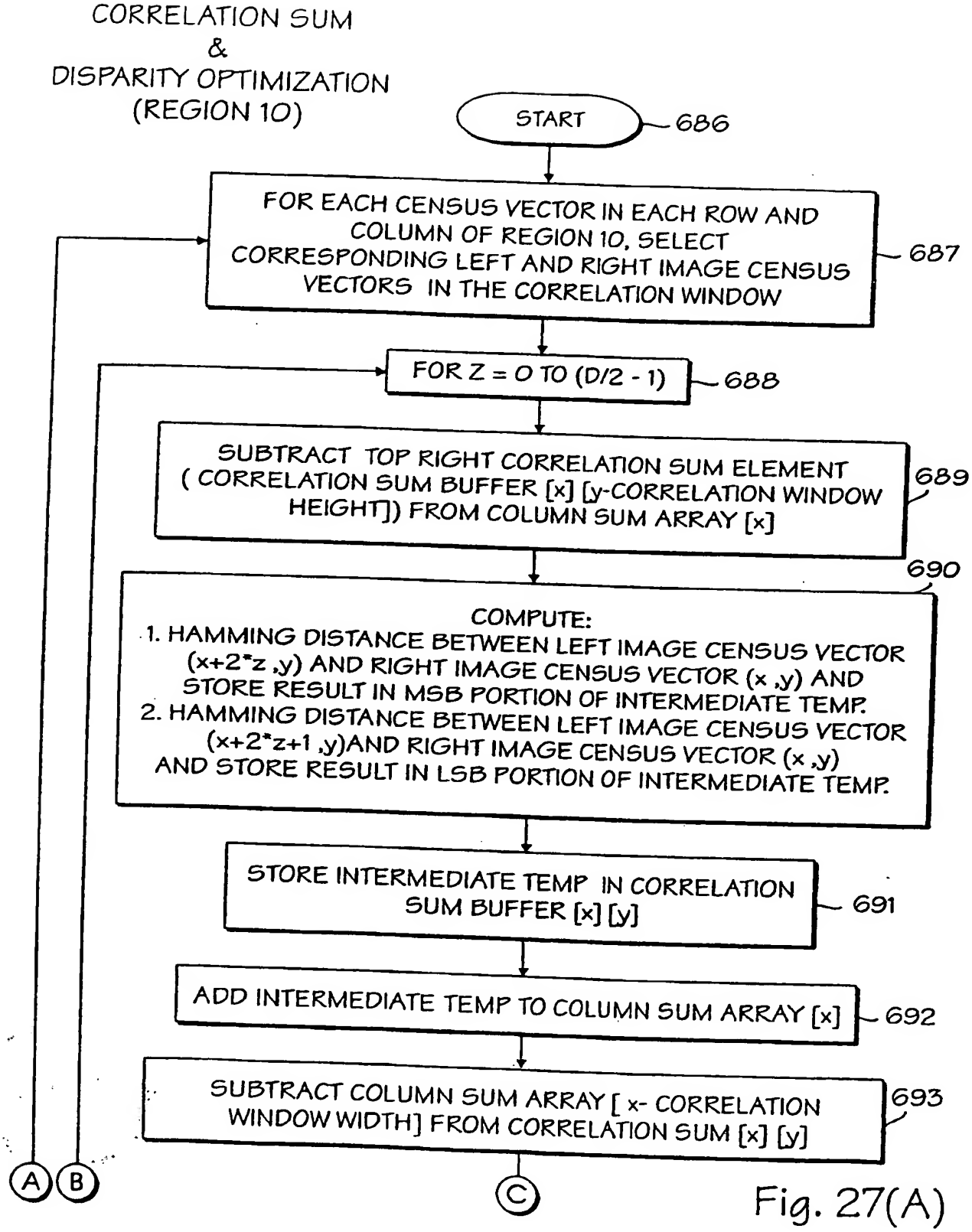
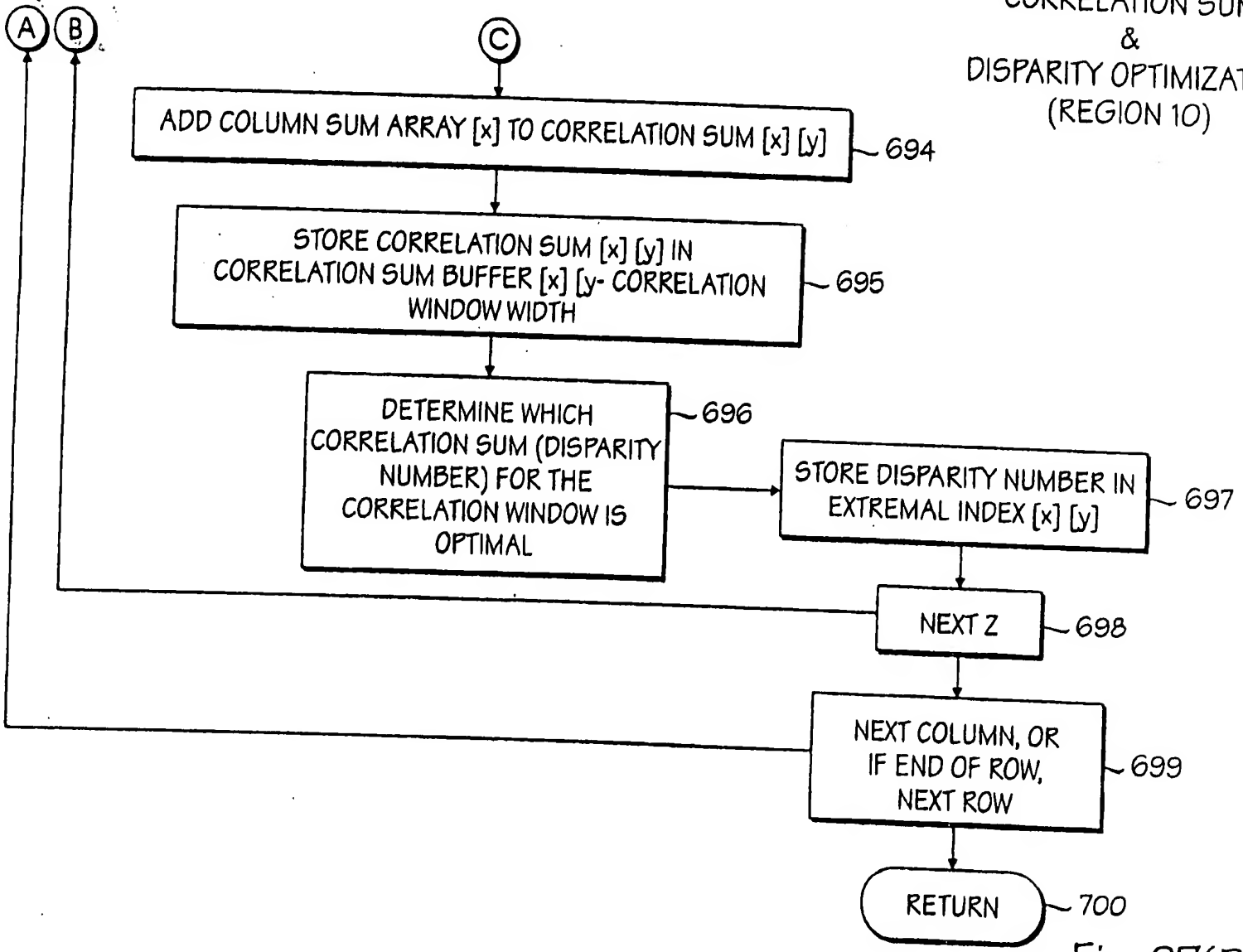

CORRELATION SUM
&
DISPARITY OPTIMIZATION
(REGION 10)
START
686
FOR EACH CENSUS VECTOR IN EACH ROW AND COLUMN OF REGION 10, SELECT CORRESPONDING LEFT AND RIGHT IMAGE CENSUS VECTORS IN THE CORRELATION WINDOW
687
FOR Z = 0 TO (D/2 - 1)
688
SUBTRACT TOP RIGHT CORRELATION SUM ELEMENT (CORRELATION SUM BUFFER [x] [y-CORRELATION WINDOW HEIGHT]) FROM COLUMN SUM ARRAY [x]
689
690
COMPUTE:
1. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z ,y) AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN MSB PORTION OF INTERMEDIATE TEMP.
2. HAMMING DISTANCE BETWEEN LEFT IMAGE CENSUS VECTOR (x+2*z+1 ,y)AND RIGHT IMAGE CENSUS VECTOR (x ,y) AND STORE RESULT IN LSB PORTION OF INTERMEDIATE TEMP.
STORE INTERMEDIATE TEMP IN CORRELATION SUM BUFFER [x] [y]
691
ADD INTERMEDIATE TEMP TO COLUMN SUM ARRAY [x]
692
SUBTRACT COLUMN SUM ARRAY [x- CORRELATION WINDOW WIDTH] FROM CORRELATION SUM [x] [y]
693
A
B
C

Fig. 27(A)



CORRELATION SUM
&
DISPARITY OPTIMIZATION
(REGION 10)

Fig. 27(B)

EP 0 762 328 A2

INTEREST OPERATION

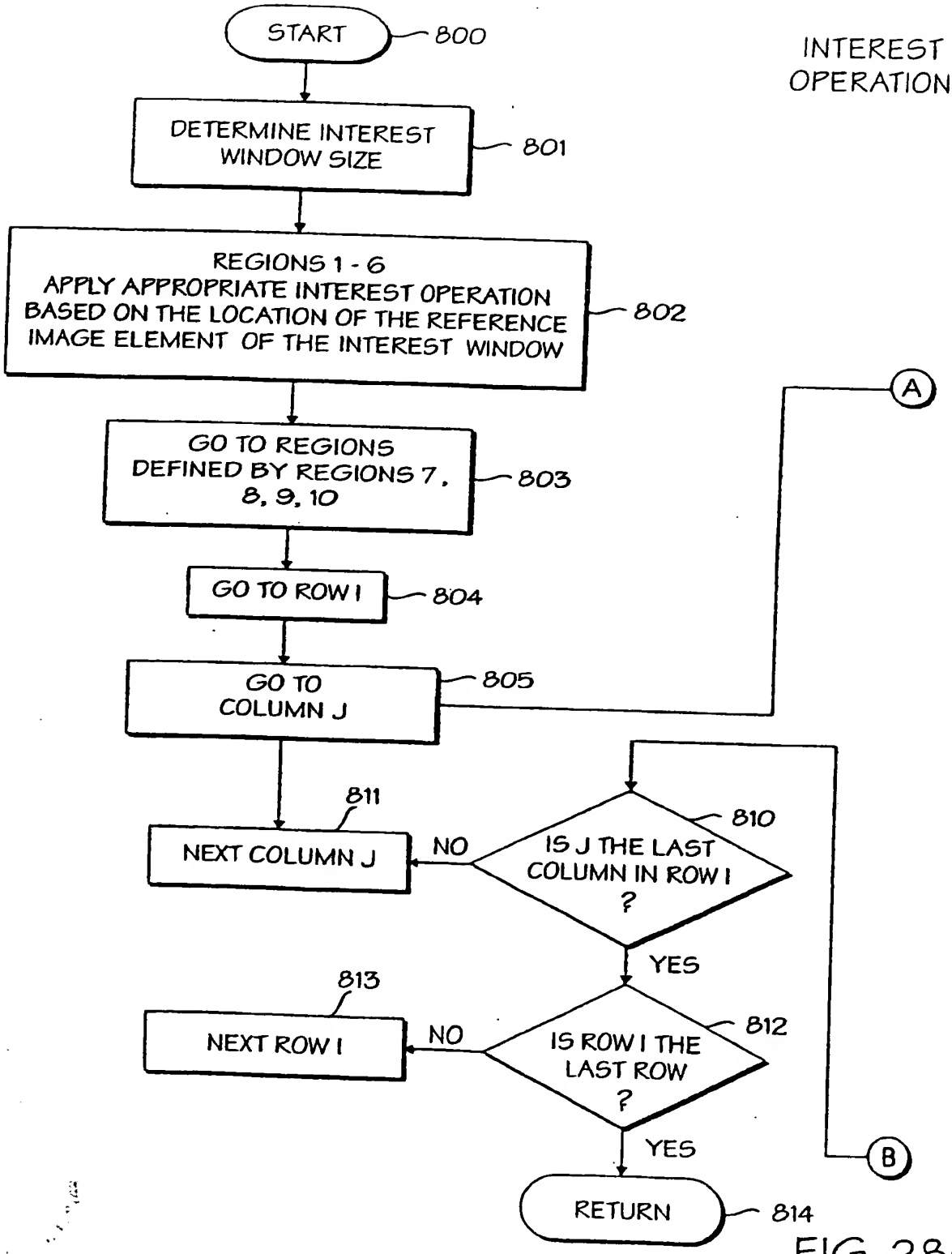


FIG. 28(A)

INTEREST
OPERATION

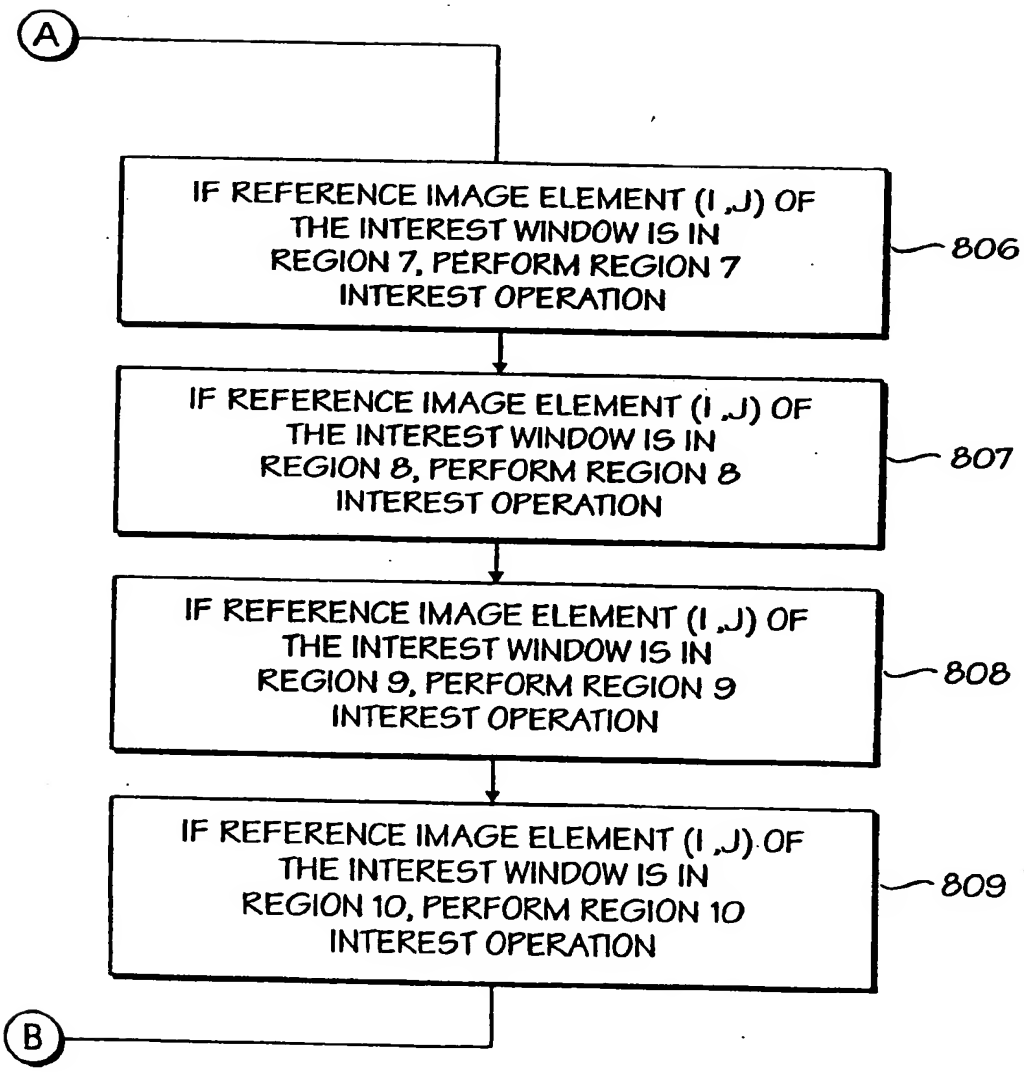


FIG 28(B)

DOCKET # 2000-0002

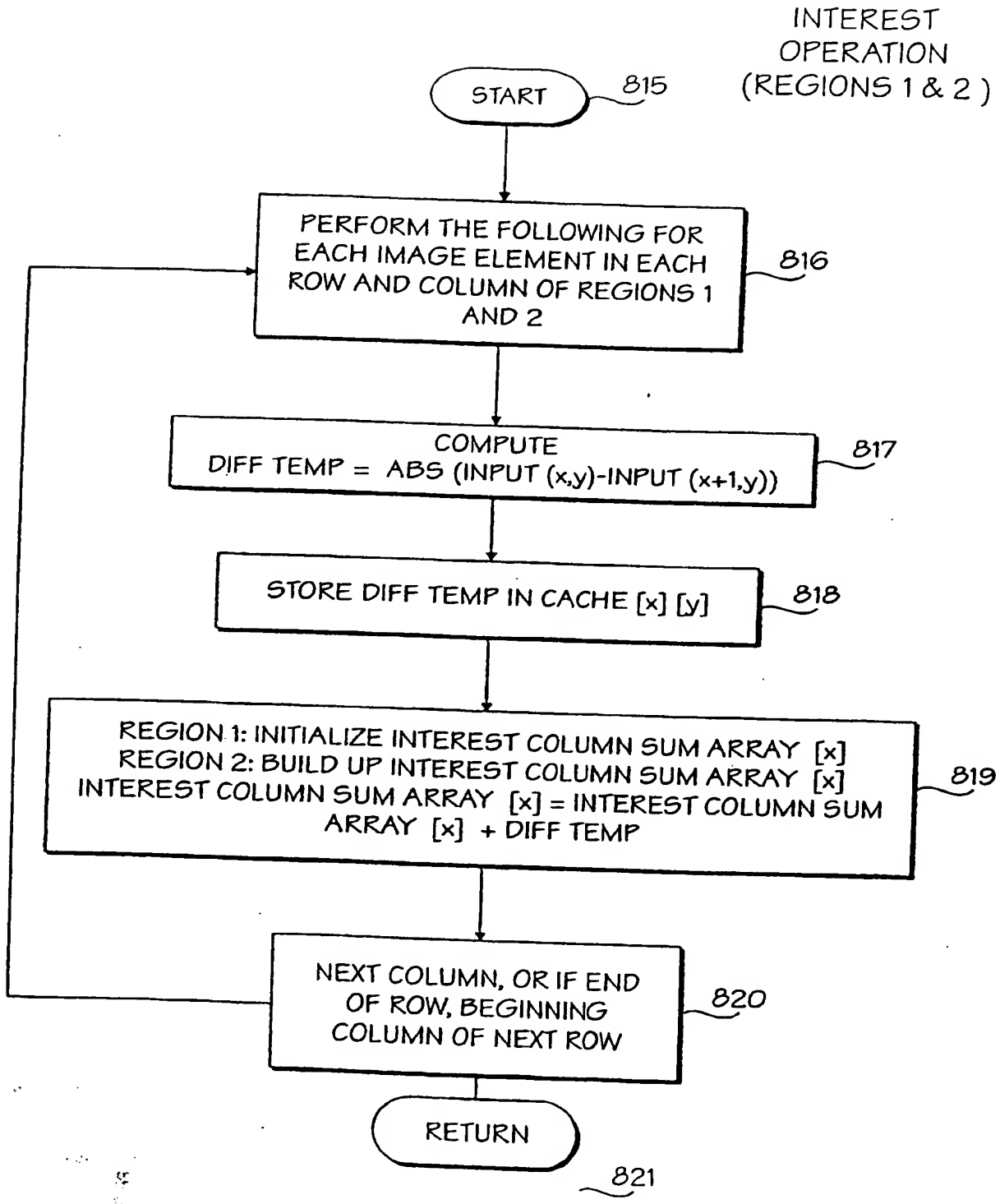


FIG. 29

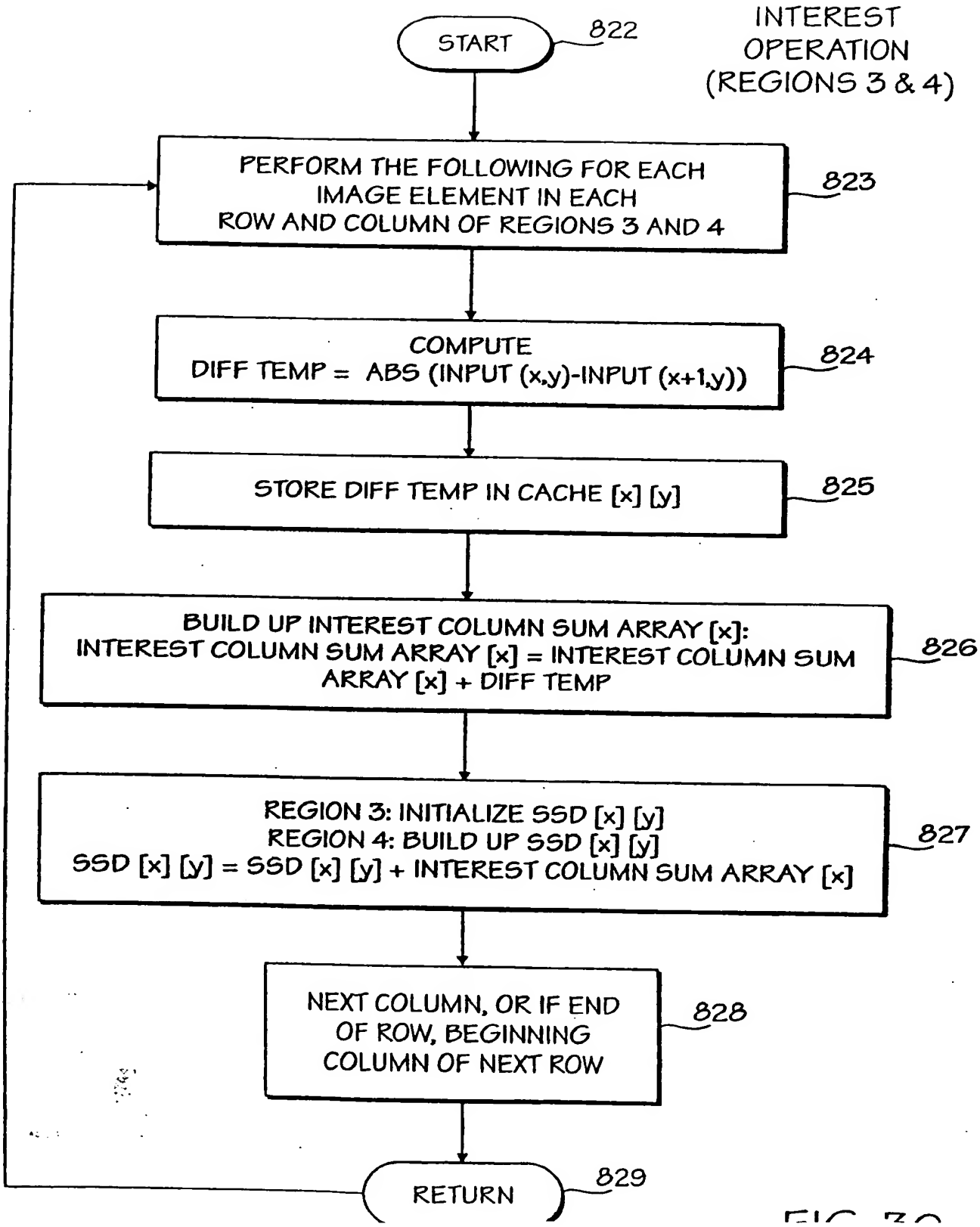

INTEREST OPERATION (REGIONS 3 & 4)
START
822
PERFORM THE FOLLOWING FOR EACH IMAGE ELEMENT IN EACH ROW AND COLUMN OF REGIONS 3 AND 4
823
COMPUTE DIFF TEMP = ABS (INPUT (x,y)-INPUT (x+1,y))
824
STORE DIFF TEMP IN CACHE [x] [y]
825
BUILD UP INTEREST COLUMN SUM ARRAY [x]: INTEREST COLUMN SUM ARRAY [x] = INTEREST COLUMN SUM ARRAY [x] + DIFF TEMP
826
REGION 3: INITIALIZE SSD [x] [y]
REGION 4: BUILD UP SSD [x] [y]
SSD [x] [y] = SSD [x] [y] + INTEREST COLUMN SUM ARRAY [x]
827
NEXT COLUMN, OR IF END OF ROW, BEGINNING COLUMN OF NEXT ROW
828
RETURN
829

FIG. 30

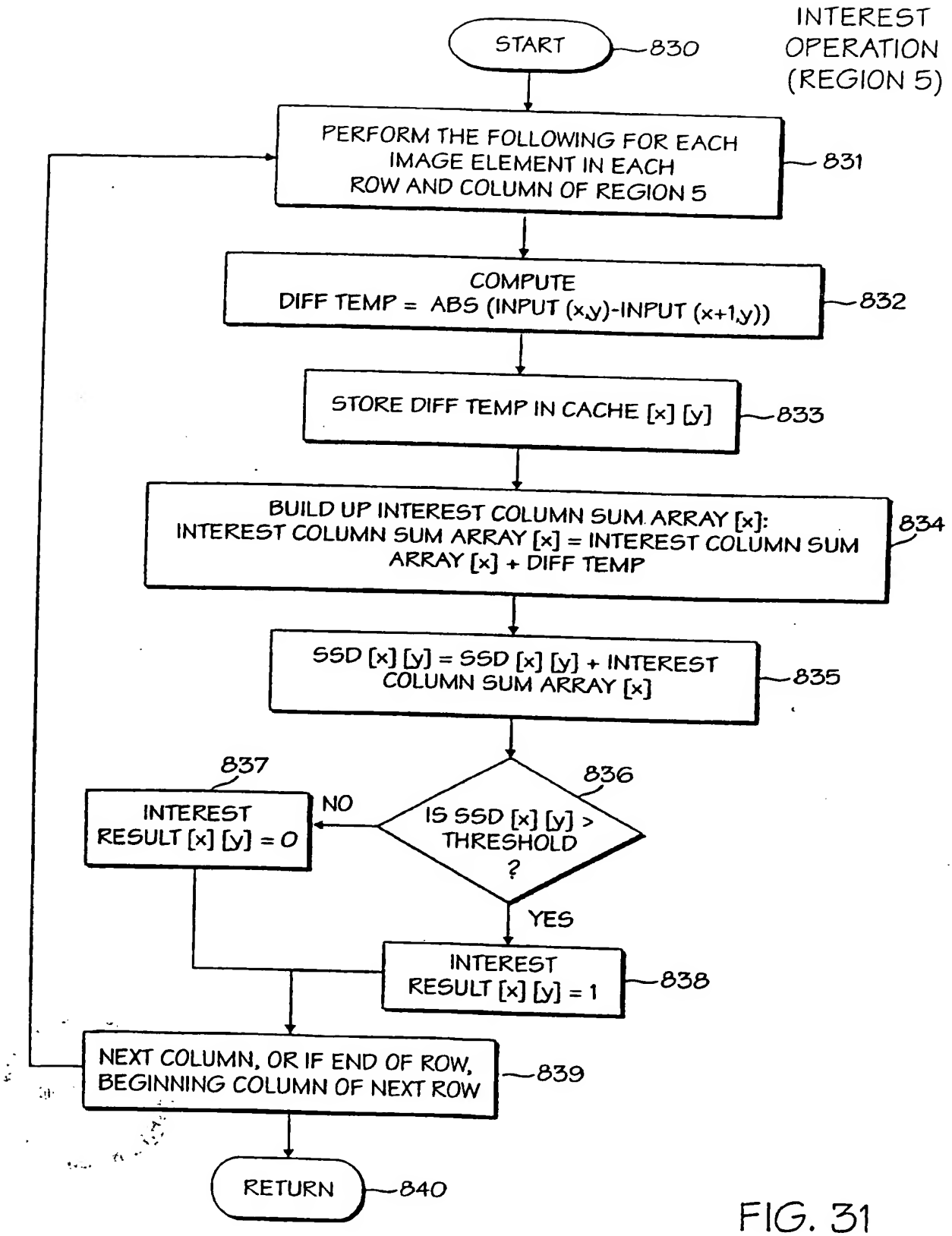

INTEREST OPERATION (REGION 5)
START
830
PERFORM THE FOLLOWING FOR EACH IMAGE ELEMENT IN EACH ROW AND COLUMN OF REGION 5
831
COMPUTE DIFF TEMP = ABS (INPUT (x,y)-INPUT (x+1,y))
832
STORE DIFF TEMP IN CACHE [x] [y]
833
BUILD UP INTEREST COLUMN SUM ARRAY [x]: INTEREST COLUMN SUM ARRAY [x] = INTEREST COLUMN SUM ARRAY [x] + DIFF TEMP
834
SSD [x] [y] = SSD [x] [y] + INTEREST COLUMN SUM ARRAY [x]
835
836
IS SSD [x] [y] > THRESHOLD ?
NO
837
INTEREST RESULT [x] [y] = 0
YES
INTEREST RESULT [x] [y] = 1
838
NEXT COLUMN, OR IF END OF ROW, BEGINNING COLUMN OF NEXT ROW
839
RETURN
840

FIG. 31

Datapoint 2500201

INTEREST OPERATION (REGION 6)

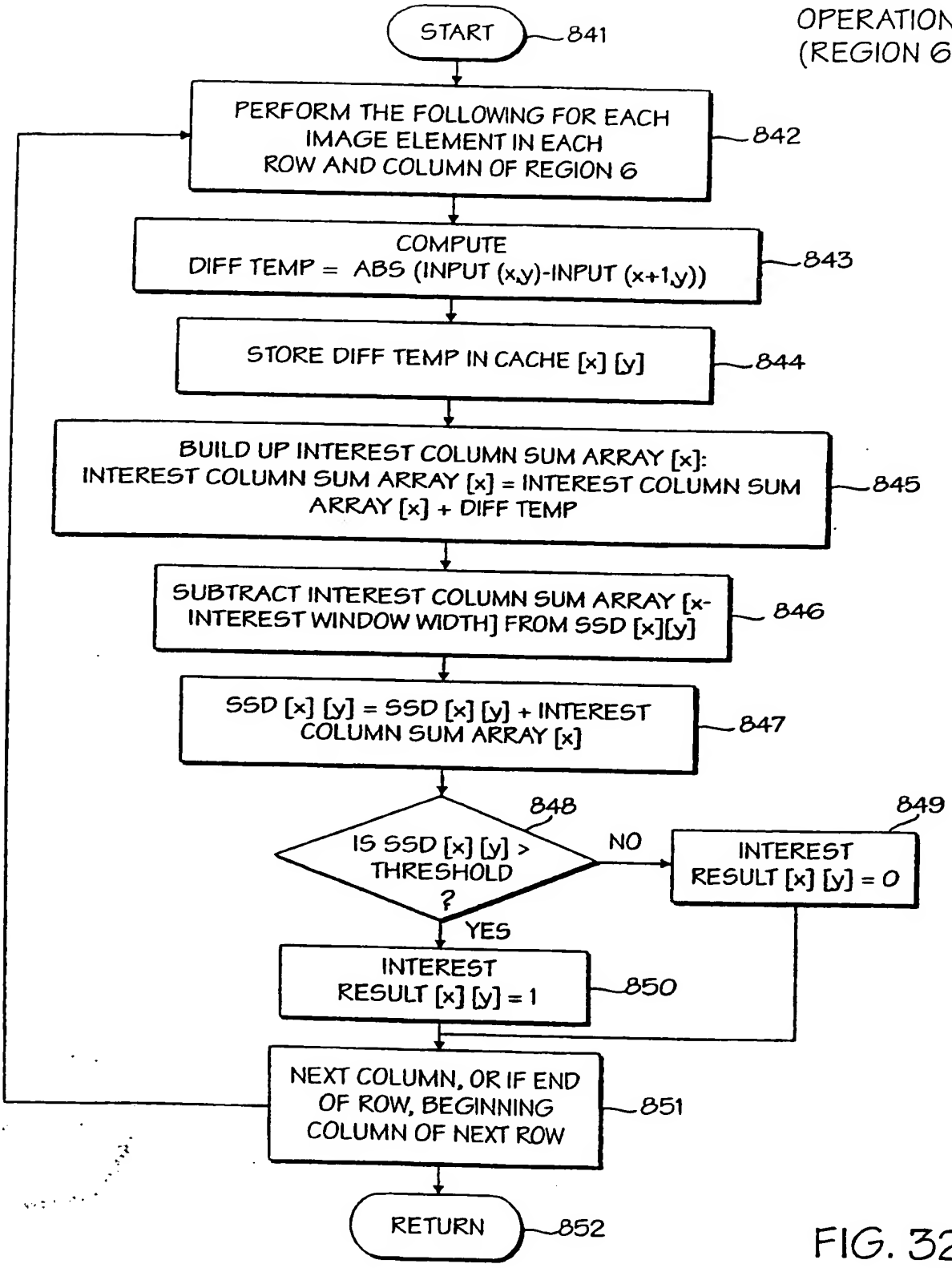


FIG. 32

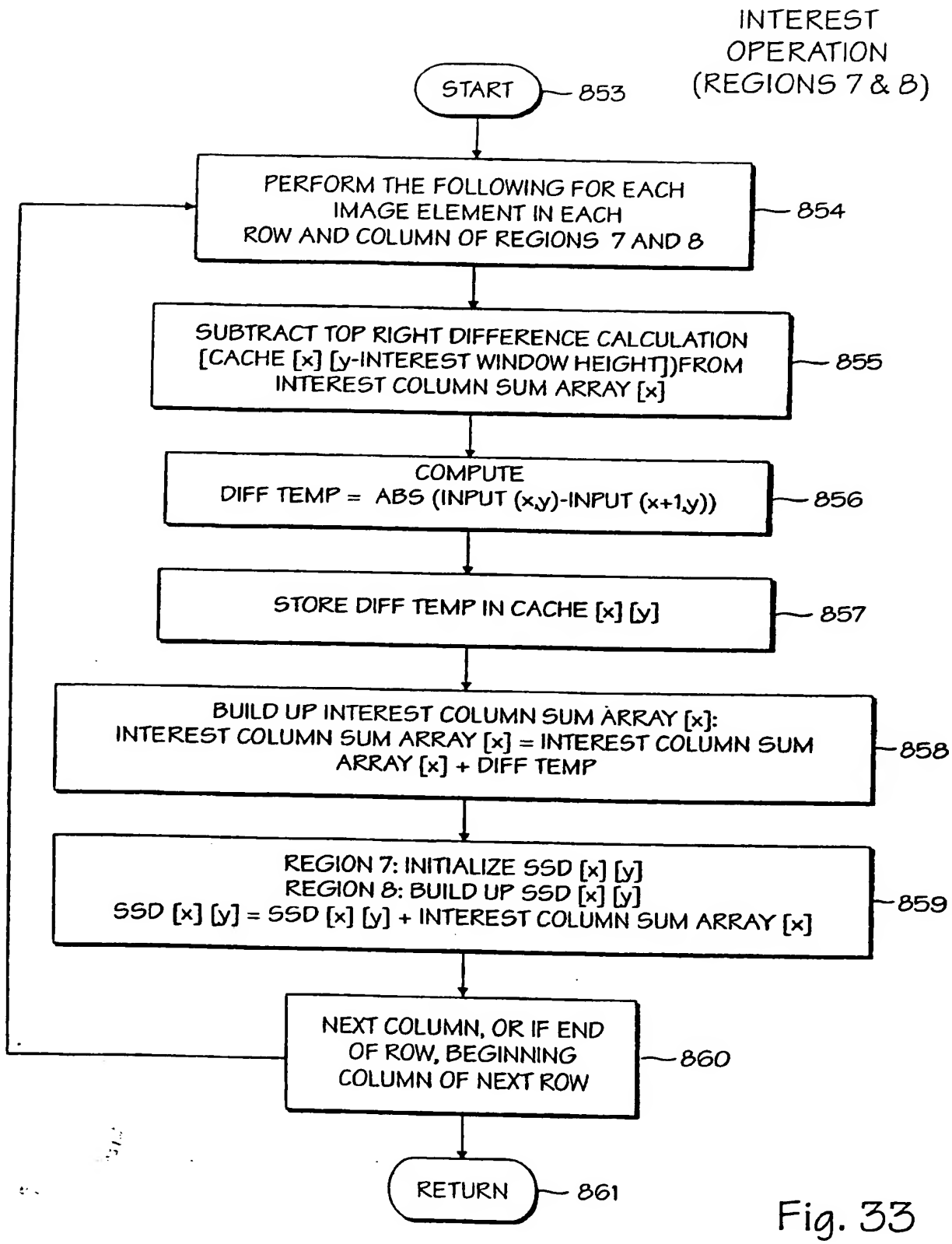

INTEREST OPERATION (REGIONS 7 & 8)
START
853
PERFORM THE FOLLOWING FOR EACH IMAGE ELEMENT IN EACH ROW AND COLUMN OF REGIONS 7 AND 8
854
SUBTRACT TOP RIGHT DIFFERENCE CALCULATION [CACHE [x] [y-INTEREST WINDOW HEIGHT])FROM INTEREST COLUMN SUM ARRAY [x]
855
COMPUTE DIFF TEMP = ABS (INPUT (x,y)-INPUT (x+1,y))
856
STORE DIFF TEMP IN CACHE [x] [y]
857
BUILD UP INTEREST COLUMN SUM ARRAY [x]: INTEREST COLUMN SUM ARRAY [x] = INTEREST COLUMN SUM ARRAY [x] + DIFF TEMP
858
REGION 7: INITIALIZE SSD [x] [y]
REGION 8: BUILD UP SSD [x] [y]
SSD [x] [y] = SSD [x] [y] + INTEREST COLUMN SUM ARRAY [x]
859
NEXT COLUMN, OR IF END OF ROW, BEGINNING COLUMN OF NEXT ROW
860
RETURN
861

Fig. 33

INTEREST OPERATION (REGION 9)

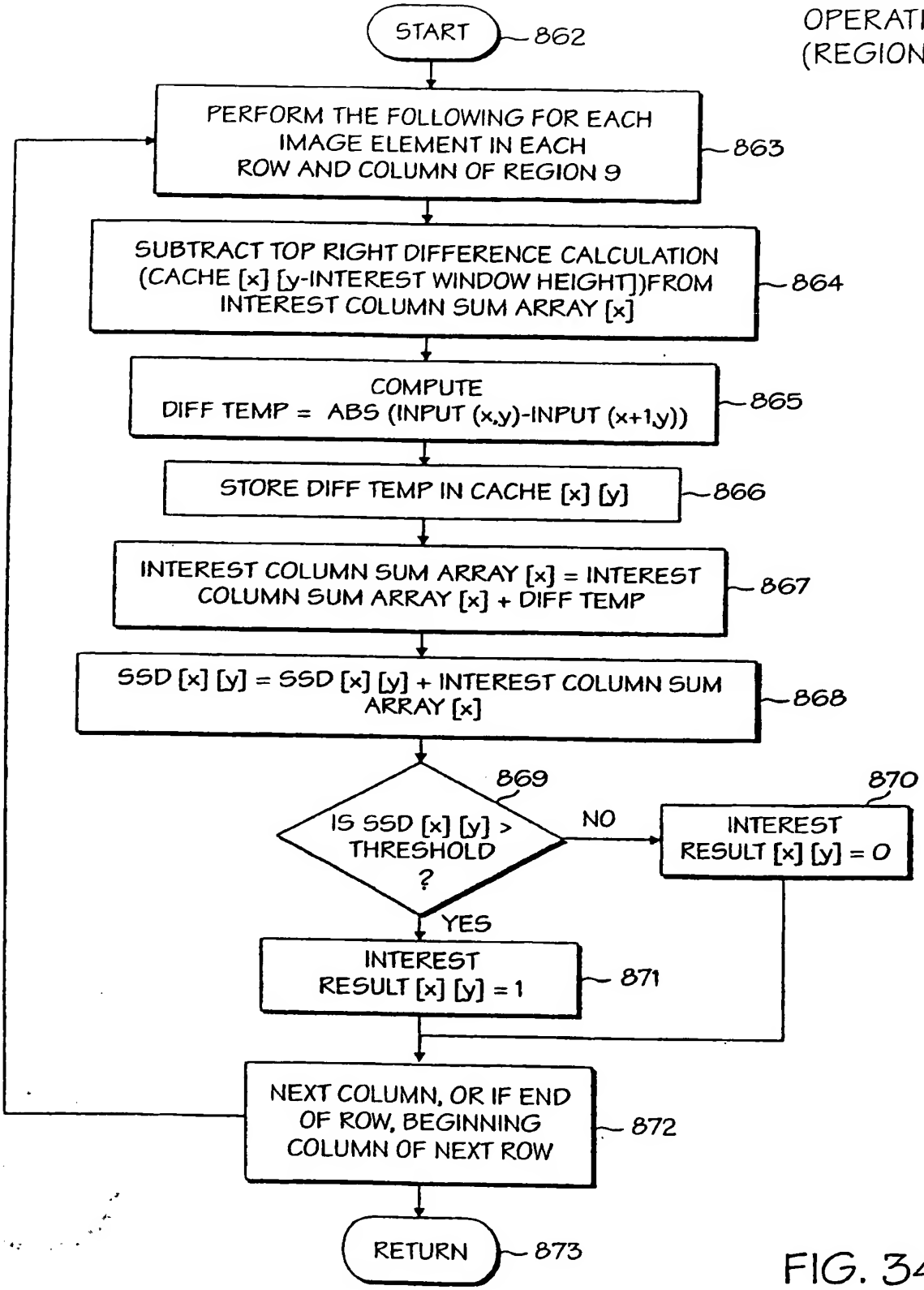


FIG. 34

INTEREST
OPERATION
(REGION 10)

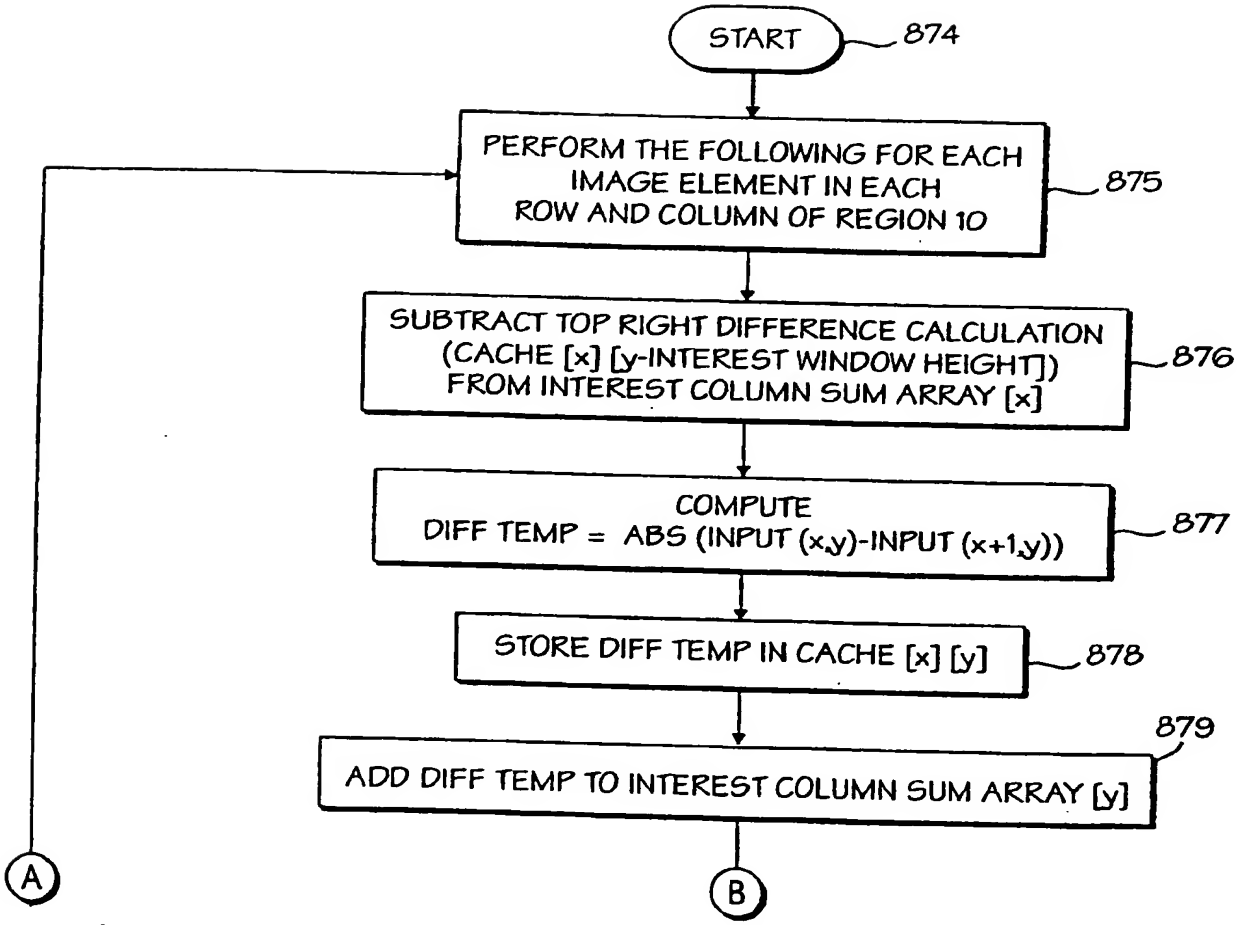


Fig. 35(A)

INTEREST
OPERATION
(REGION 10)

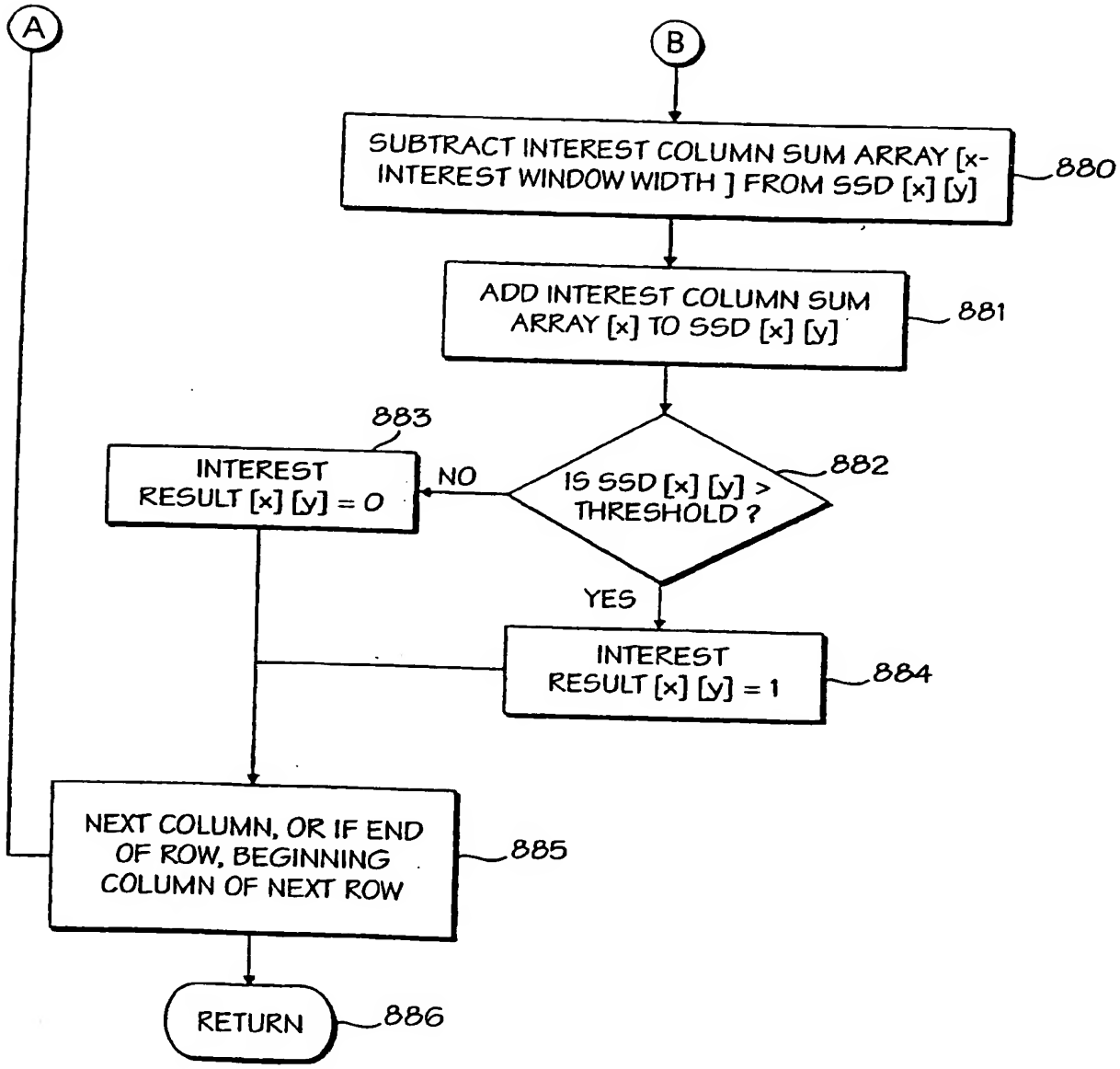


Fig. 35(B)

DETAILED DESCRIPTION

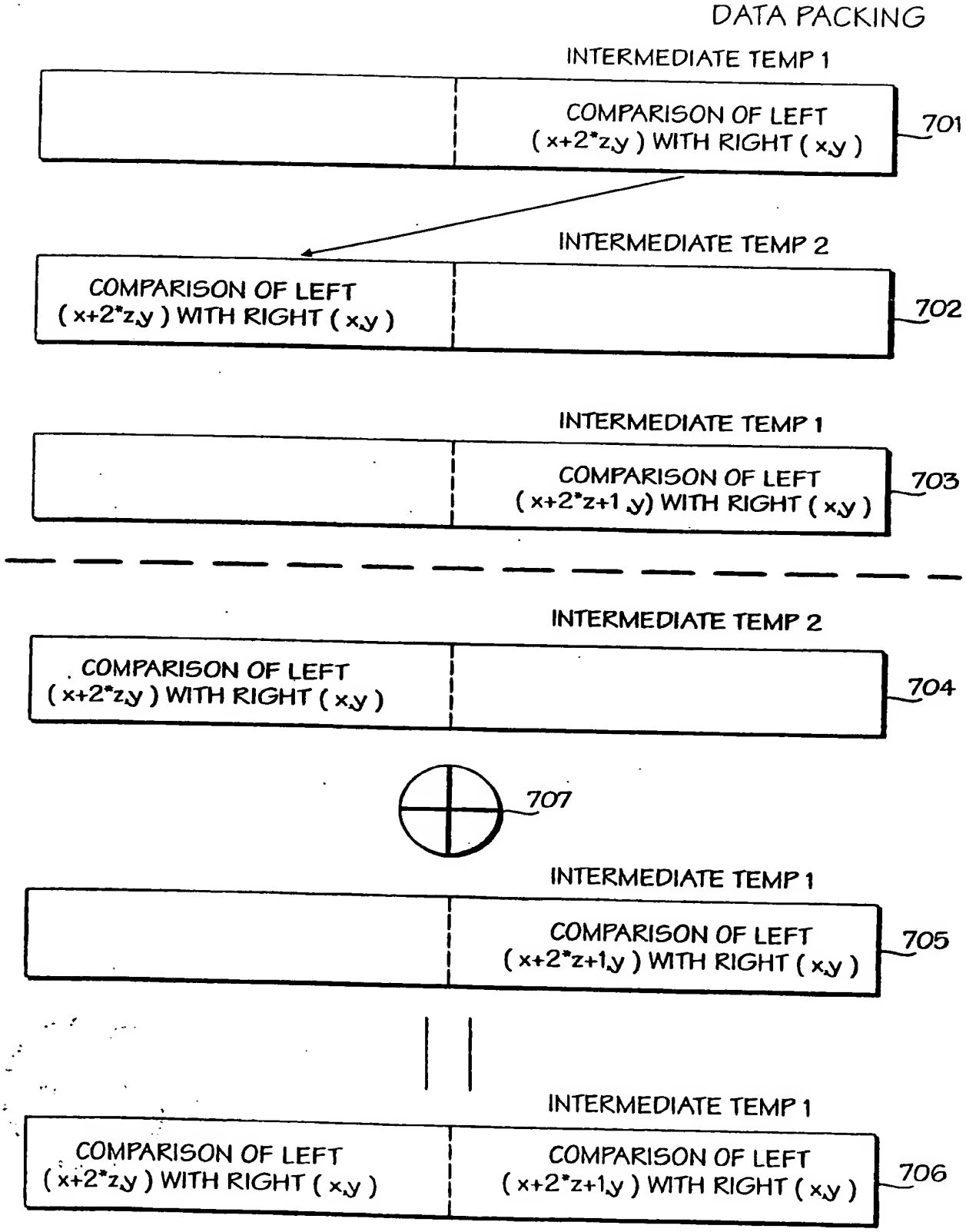


FIG 3C

LEFT - RIGHT CONSISTENCY CHECK

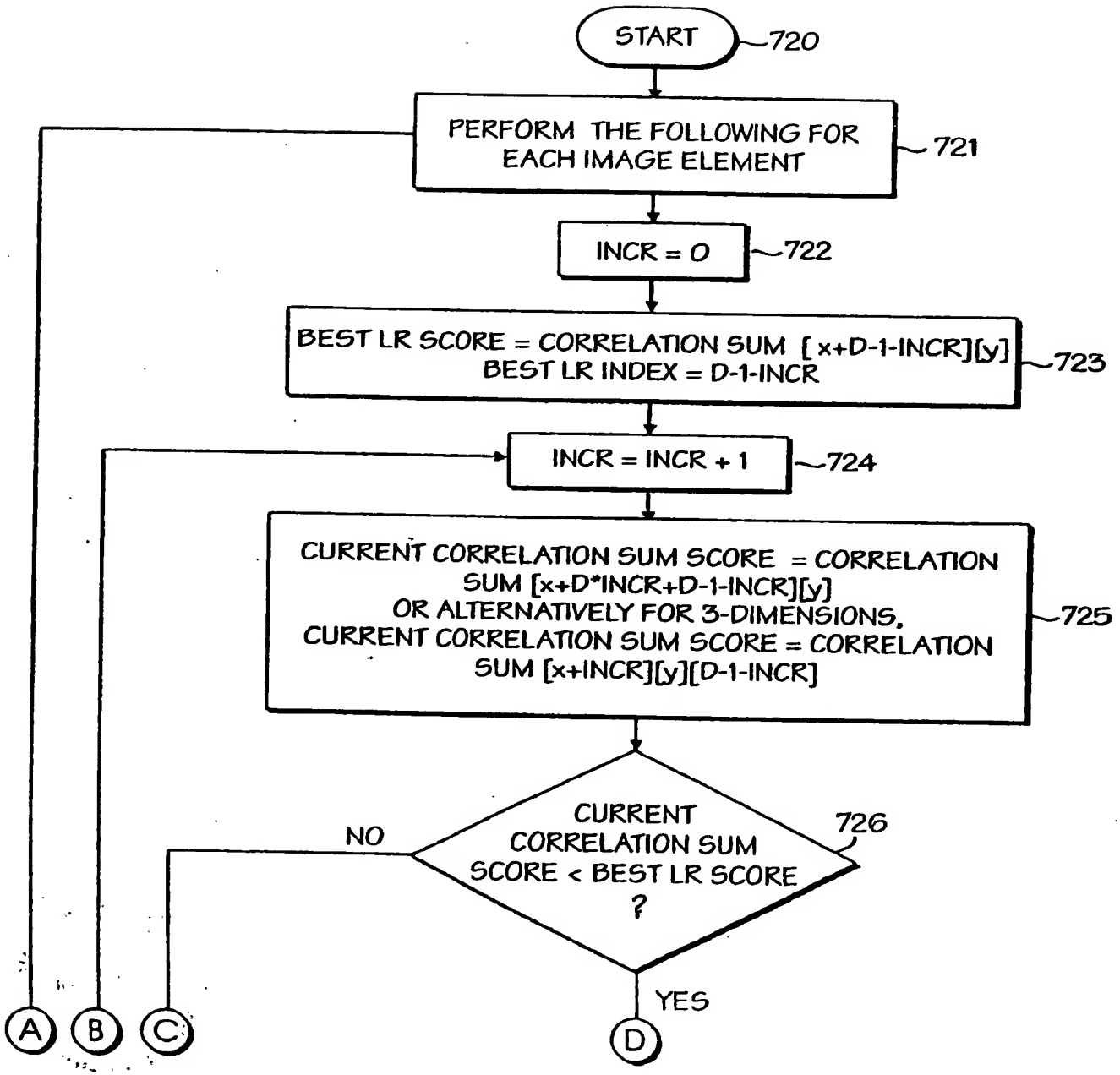
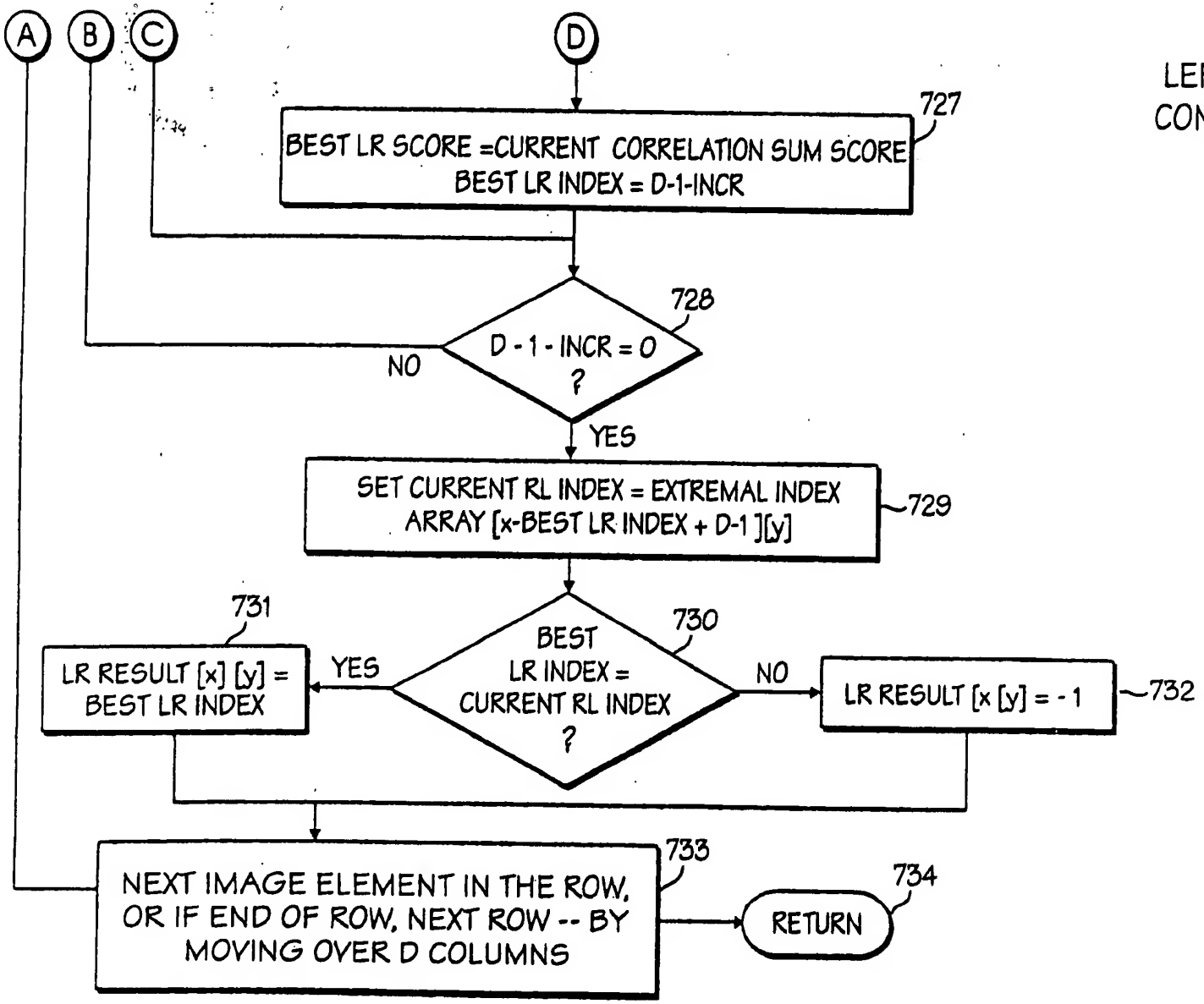


FIG. 37(A)



LEFT - RIGHT CONSISTENCY CHECK

FIG. 37(B)

DOCKET NO. 2580.2001

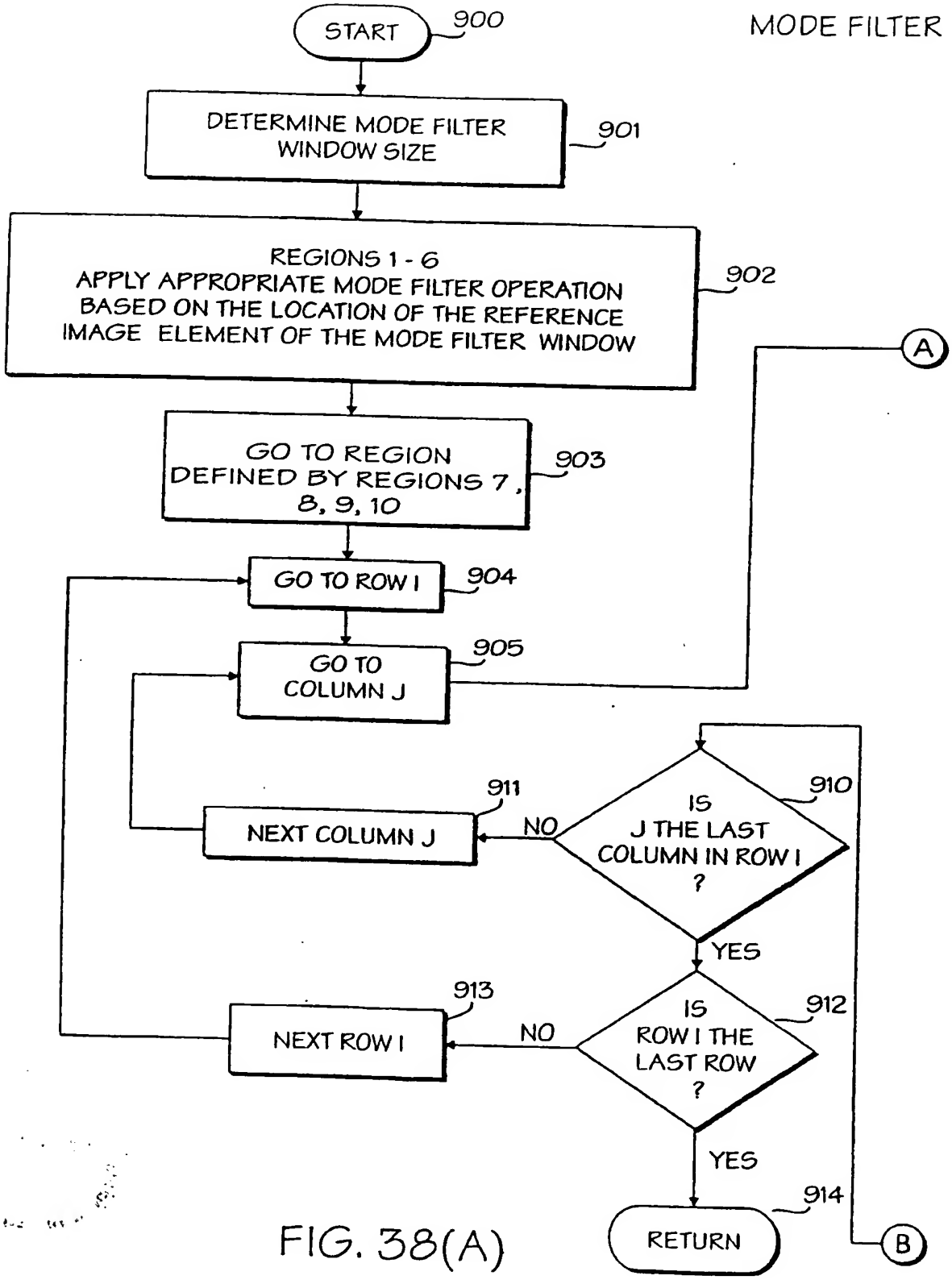


FIG. 38(A)

MODE FILTER

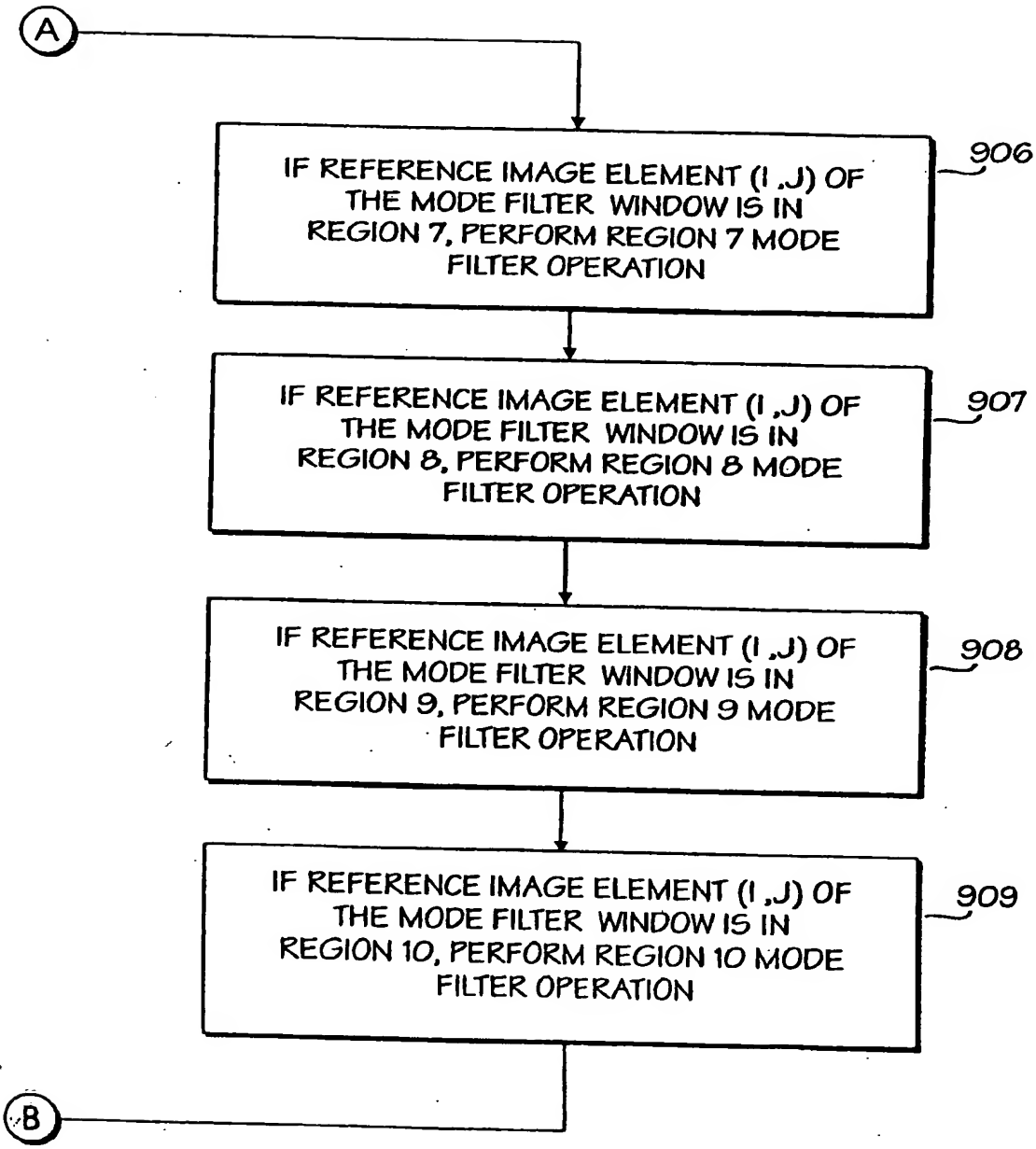


FIG. 38(B)

MODE FILTER
(REGIONS 1 & 2)

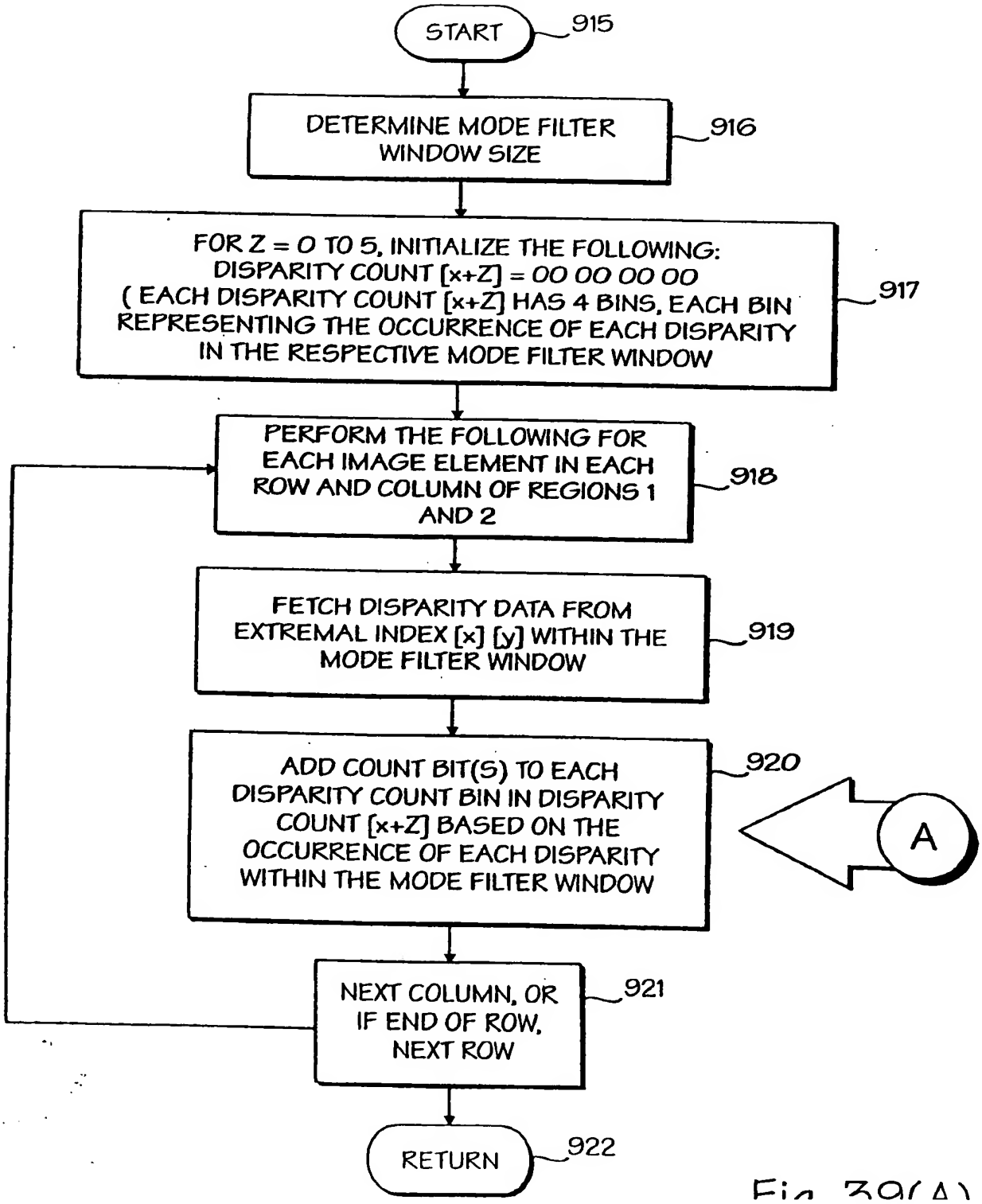


Fig 39(A)

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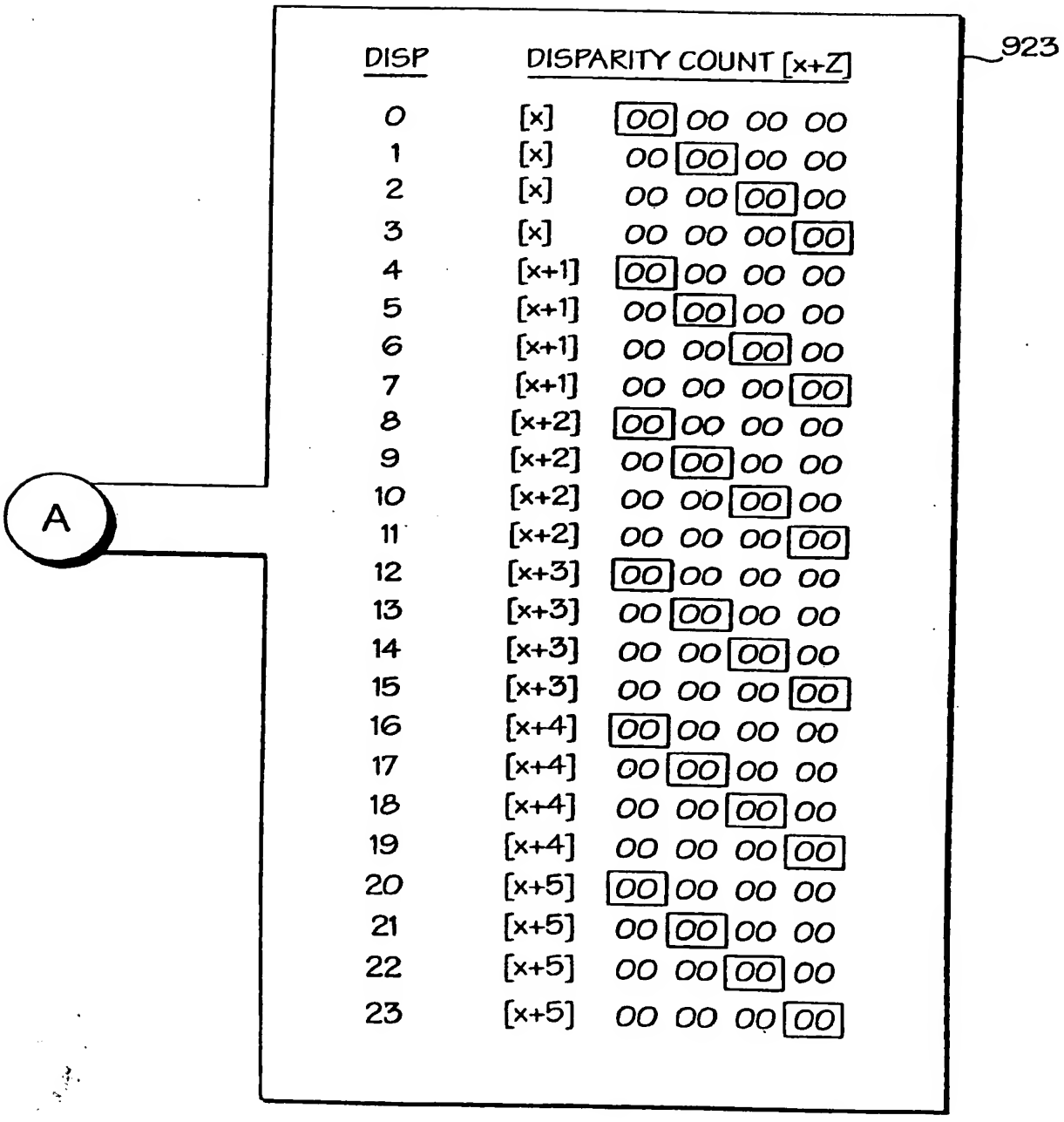
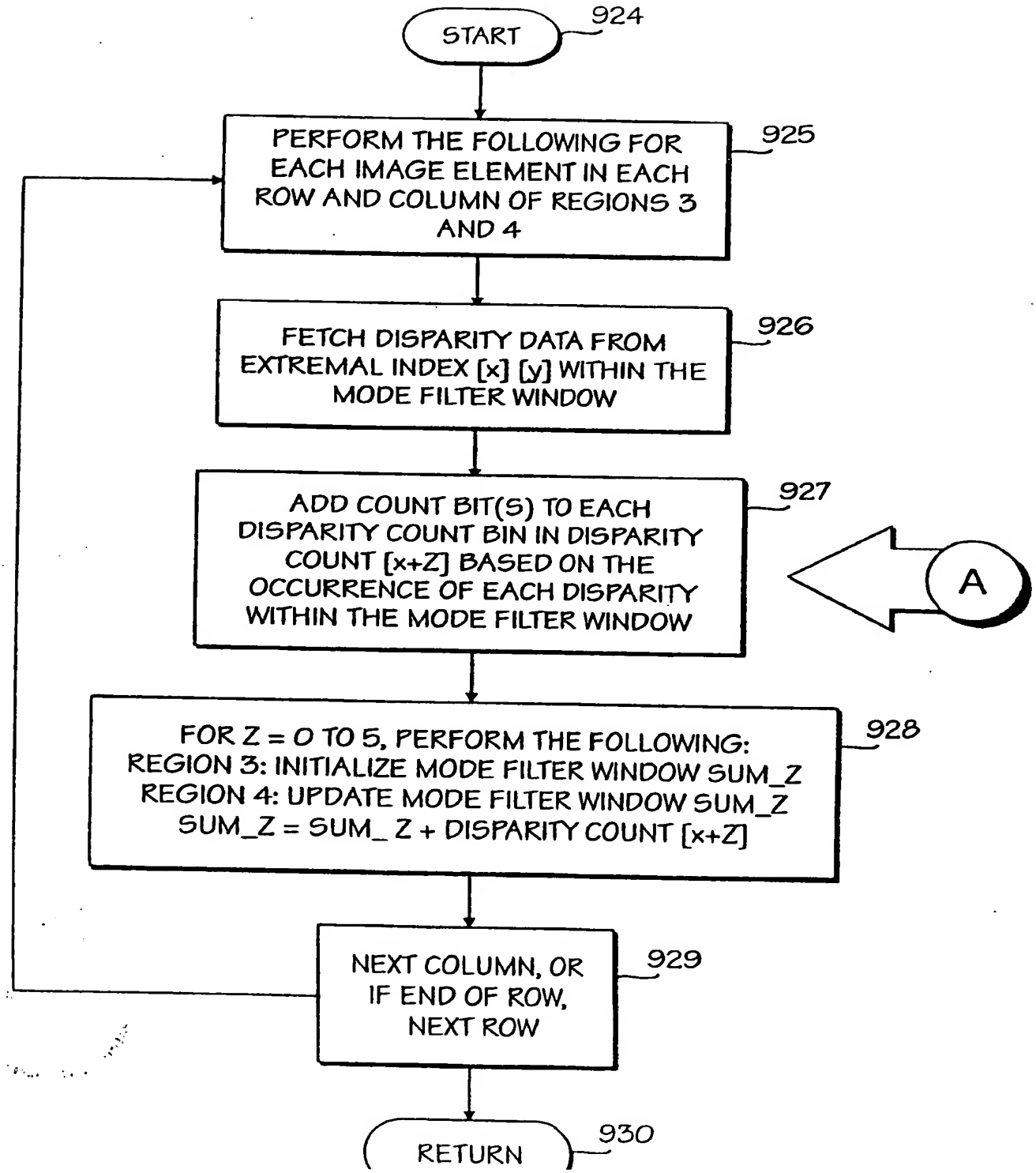
MODE FILTER
(REGIONS 1 & 2)



DISP	DISPARITY COUNT [x+Z]	
0	[x]	[00] 00 00 00
1	[x]	00 [00] 00 00
2	[x]	00 00 [00] 00
3	[x]	00 00 00 [00]
4	[x+1]	[00] 00 00 00
5	[x+1]	00 [00] 00 00
6	[x+1]	00 00 [00] 00
7	[x+1]	00 00 00 [00]
8	[x+2]	[00] 00 00 00
9	[x+2]	00 [00] 00 00
10	[x+2]	00 00 [00] 00
11	[x+2]	00 00 00 [00]
12	[x+3]	[00] 00 00 00
13	[x+3]	00 [00] 00 00
14	[x+3]	00 00 [00] 00
15	[x+3]	00 00 00 [00]
16	[x+4]	[00] 00 00 00
17	[x+4]	00 [00] 00 00
18	[x+4]	00 00 [00] 00
19	[x+4]	00 00 00 [00]
20	[x+5]	[00] 00 00 00
21	[x+5]	00 [00] 00 00
22	[x+5]	00 00 [00] 00
23	[x+5]	00 00 00 [00]

Fig 39(B)

MODE FILTER
(REGIONS 3 & 4)



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MODE FILTER
(REGIONS 3 & 4)

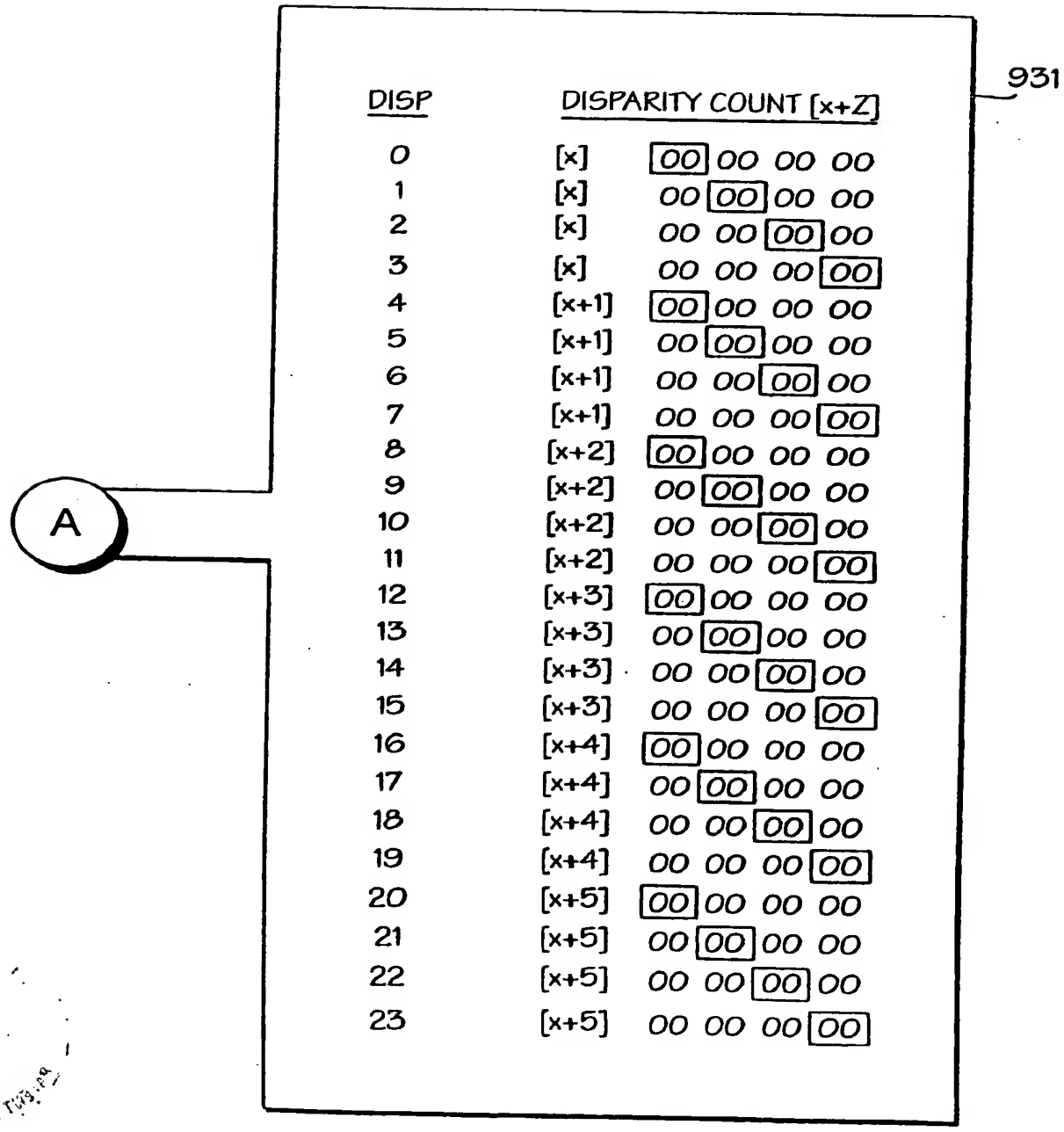


FIG 40(B)

MODE FILTER
(REGION 5)

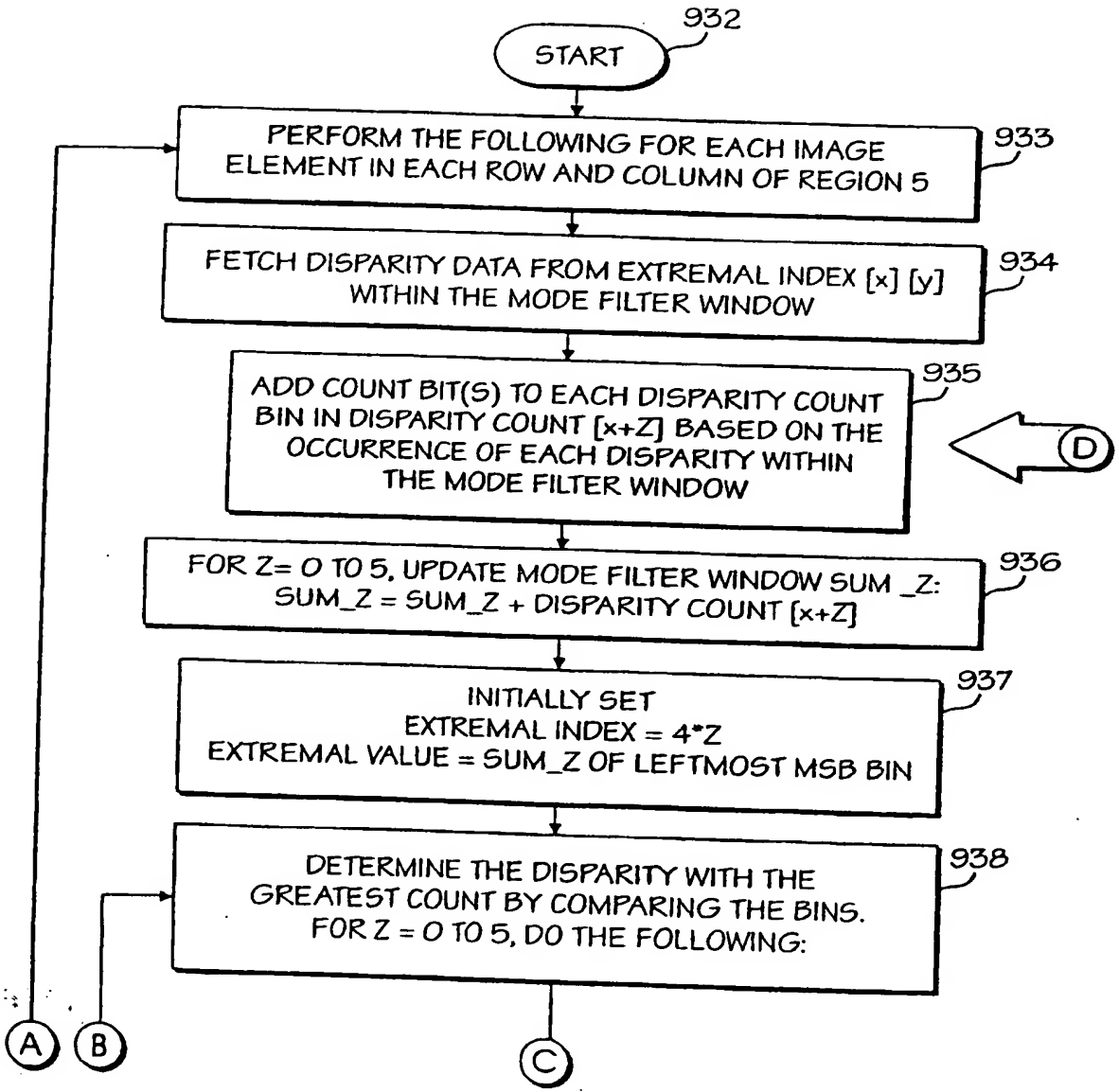
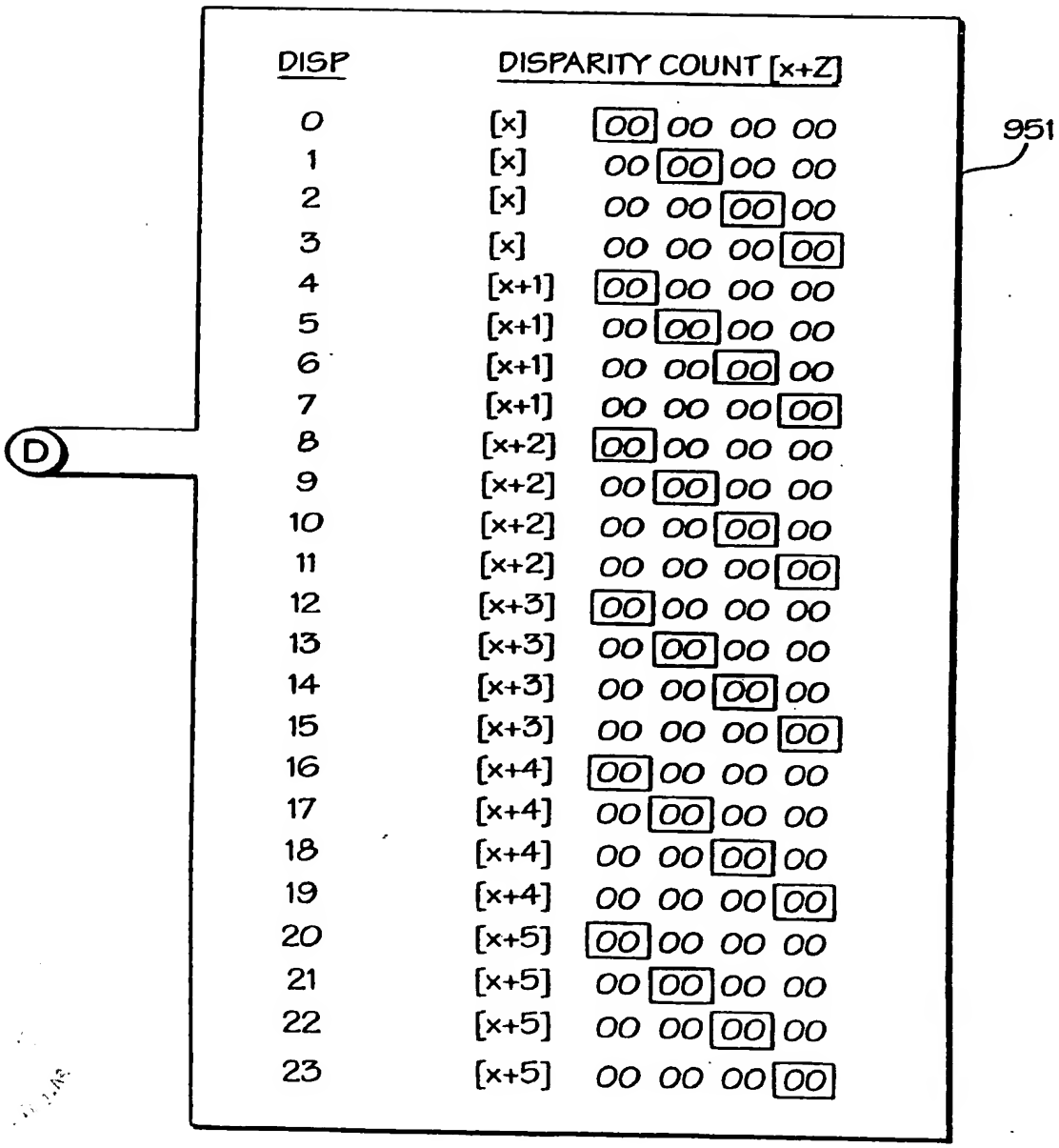


FIG. 41(A)

MODE FILTER
(REGION 5)



DISP		DISPARITY COUNT [x+Z]
0	[x]	[00] 00 00 00
1	[x]	00 [00] 00 00
2	[x]	00 00 [00] 00
3	[x]	00 00 00 [00]
4	[x+1]	[00] 00 00 00
5	[x+1]	00 [00] 00 00
6	[x+1]	00 00 [00] 00
7	[x+1]	00 00 00 [00]
8	[x+2]	[00] 00 00 00
9	[x+2]	00 [00] 00 00
10	[x+2]	00 00 [00] 00
11	[x+2]	00 00 00 [00]
12	[x+3]	[00] 00 00 00
13	[x+3]	00 [00] 00 00
14	[x+3]	00 00 [00] 00
15	[x+3]	00 00 00 [00]
16	[x+4]	[00] 00 00 00
17	[x+4]	00 [00] 00 00
18	[x+4]	00 00 [00] 00
19	[x+4]	00 00 00 [00]
20	[x+5]	[00] 00 00 00
21	[x+5]	00 [00] 00 00
22	[x+5]	00 00 [00] 00
23	[x+5]	00 00 00 [00]

FIG. 41(B)

20170260 - 29302001

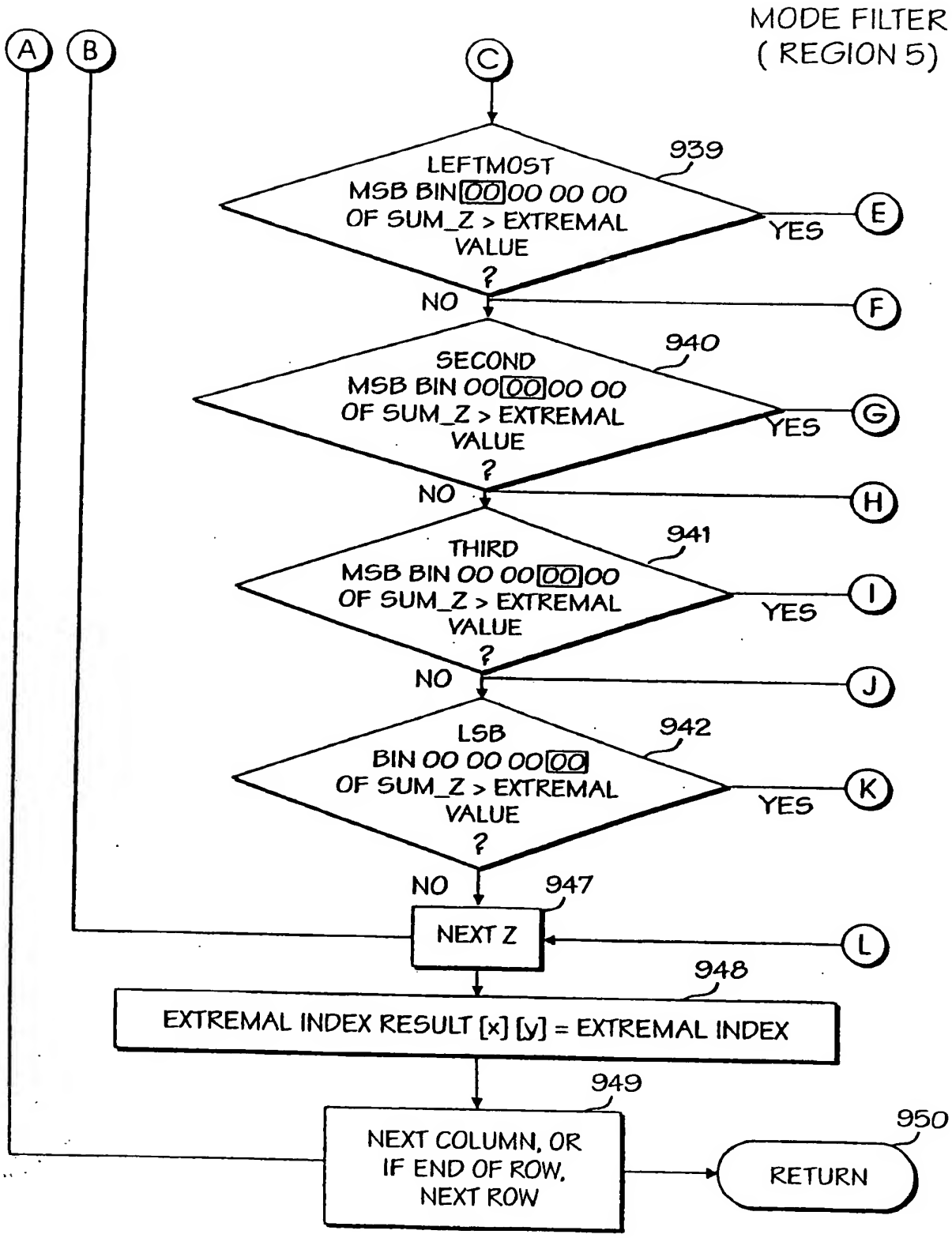


FIG. 41(C)

MODE FILTER
(REGION 5)

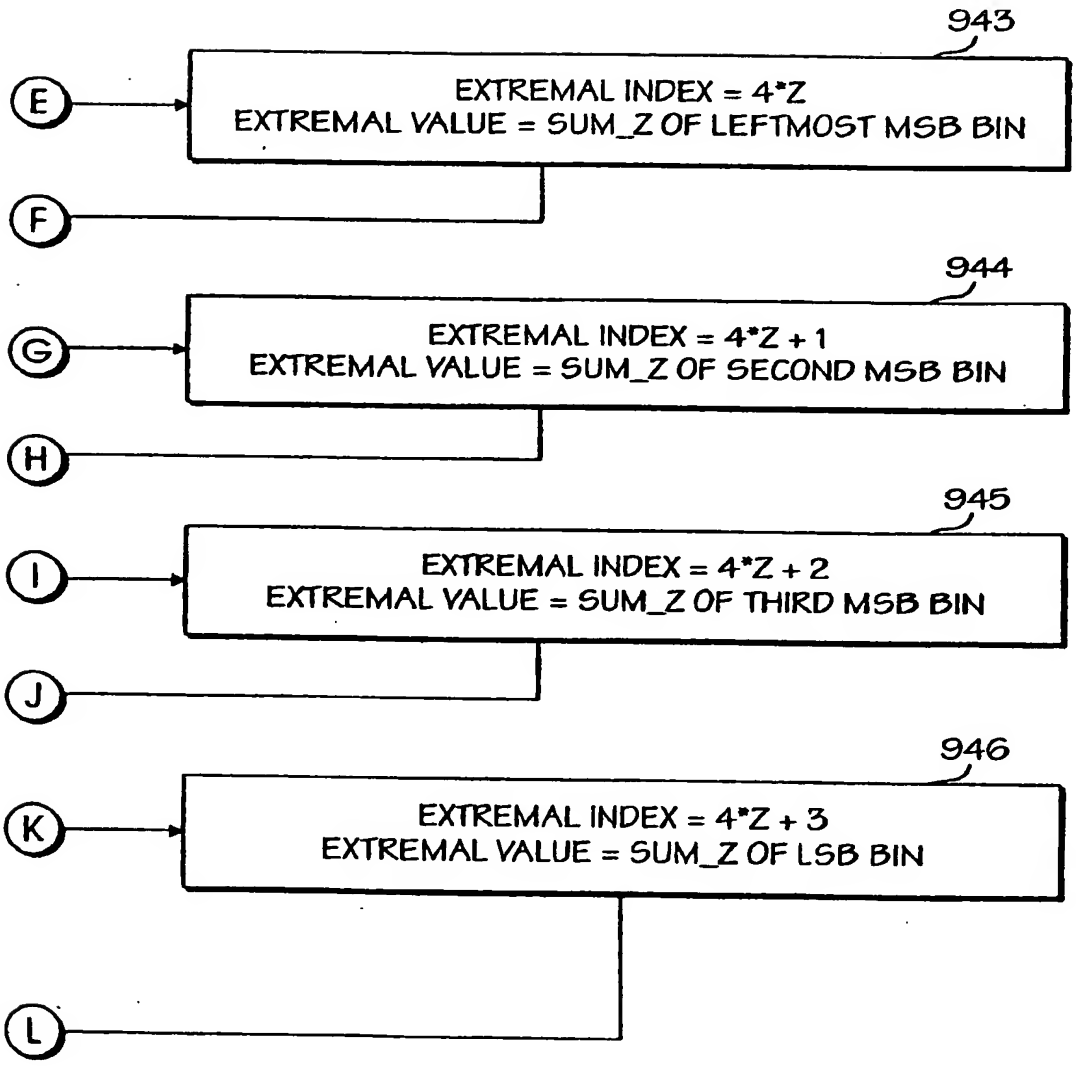


FIG. 41(D)

EXHIBIT 1008 - 0202

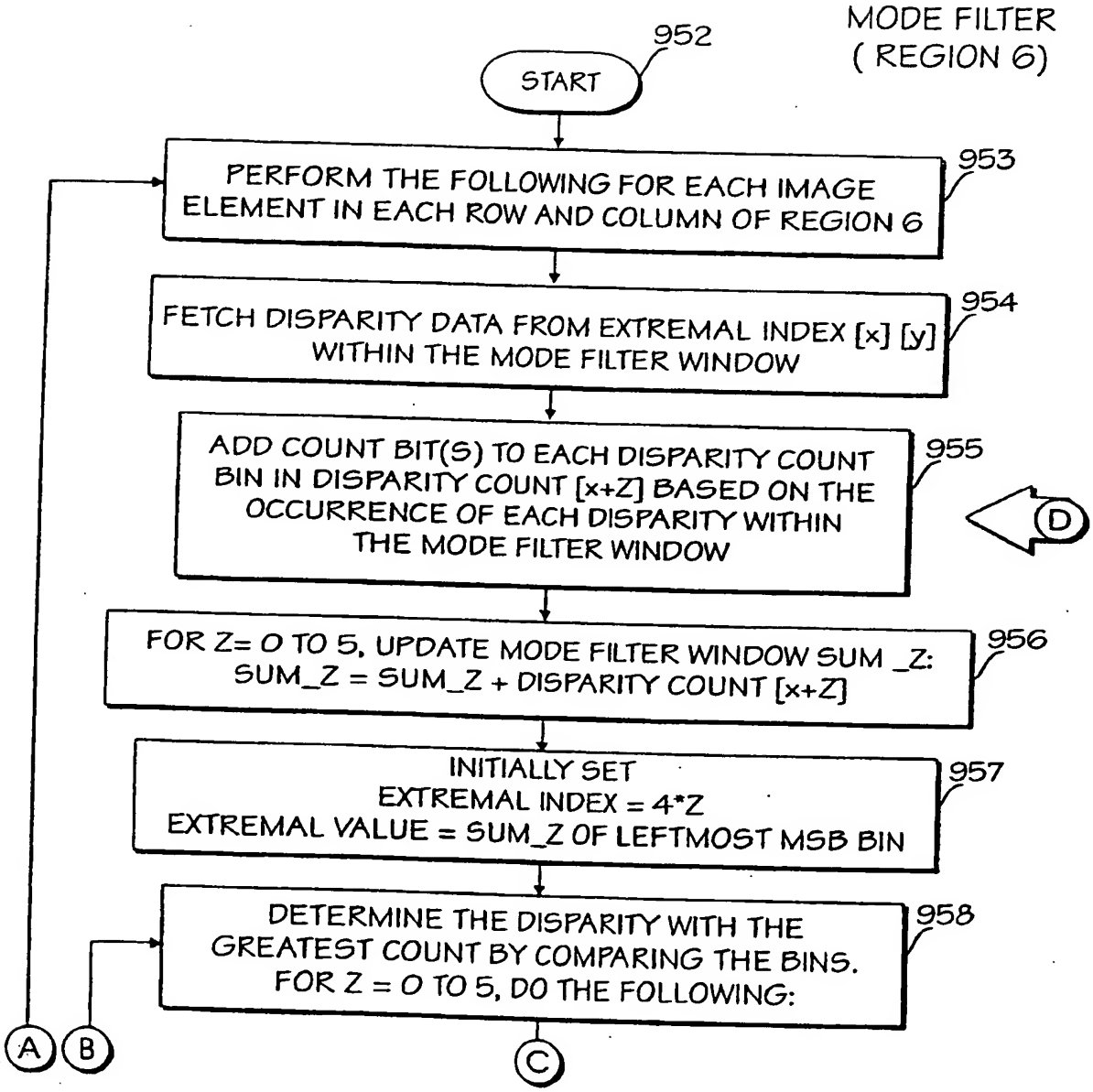


FIG. 42(A)

MODE FILTER
(REGION 6)

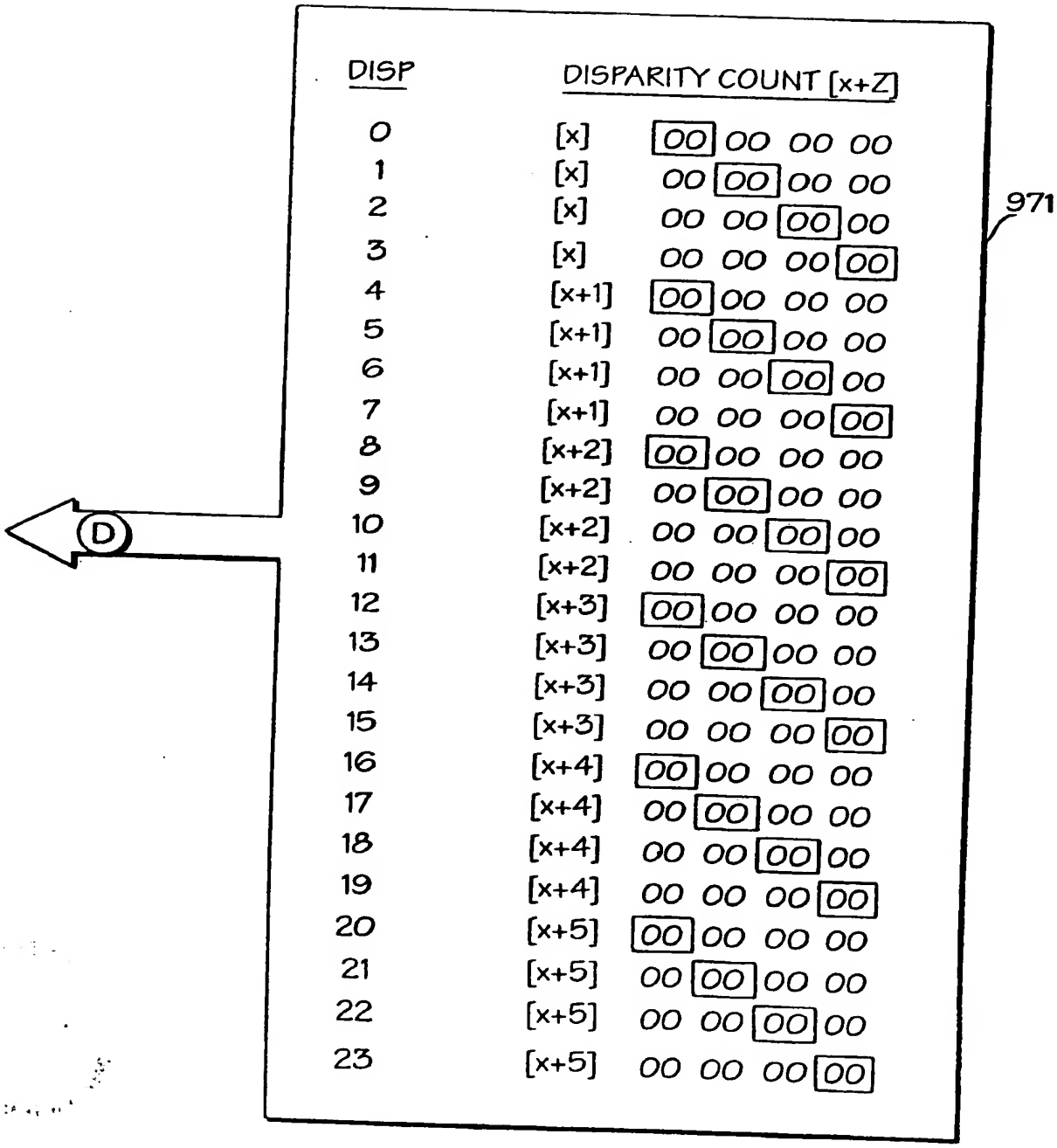


FIG. 12(B)

Patent Application Publication

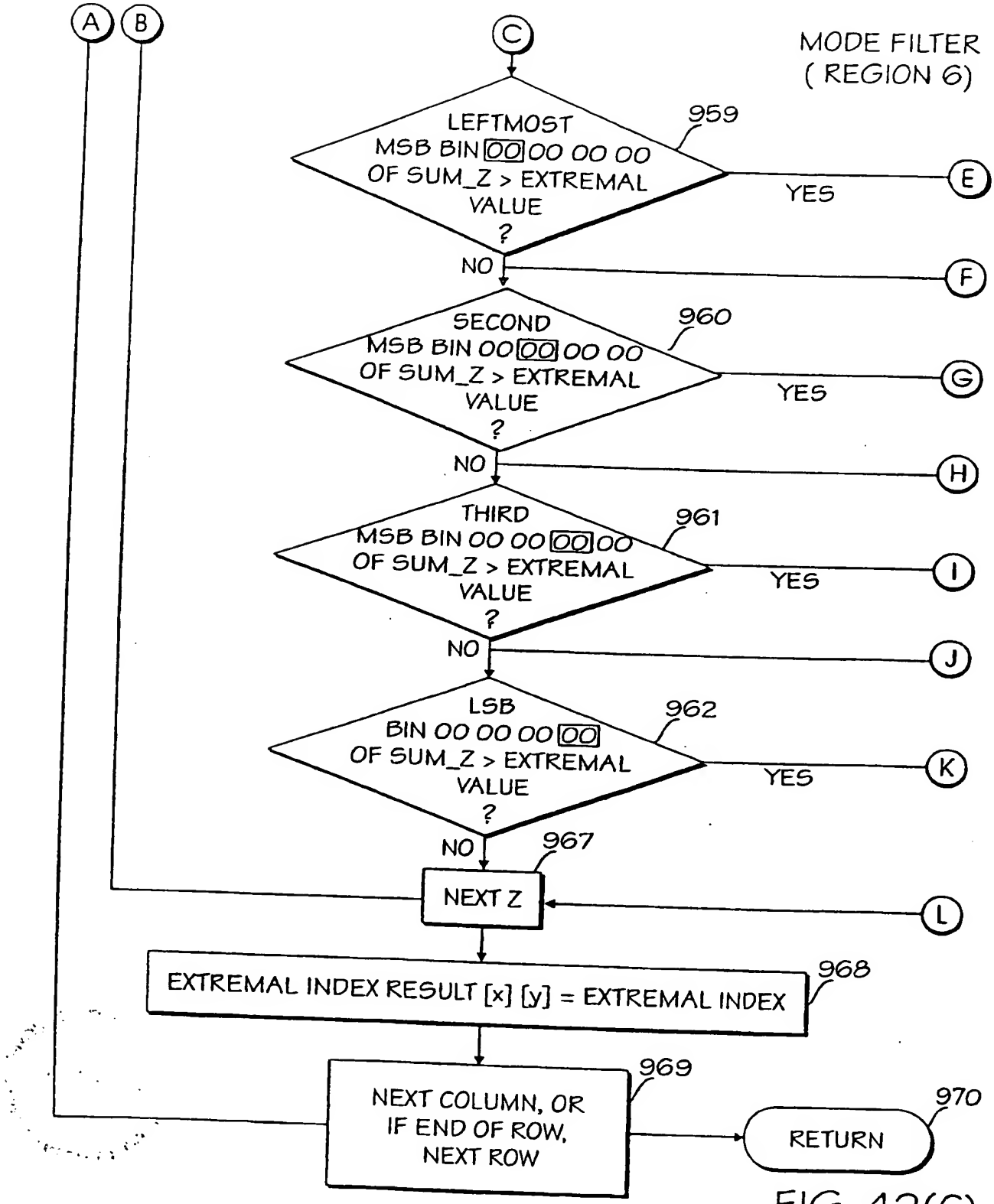


FIG. 42(C)

MODE FILTER
(REGION 6)

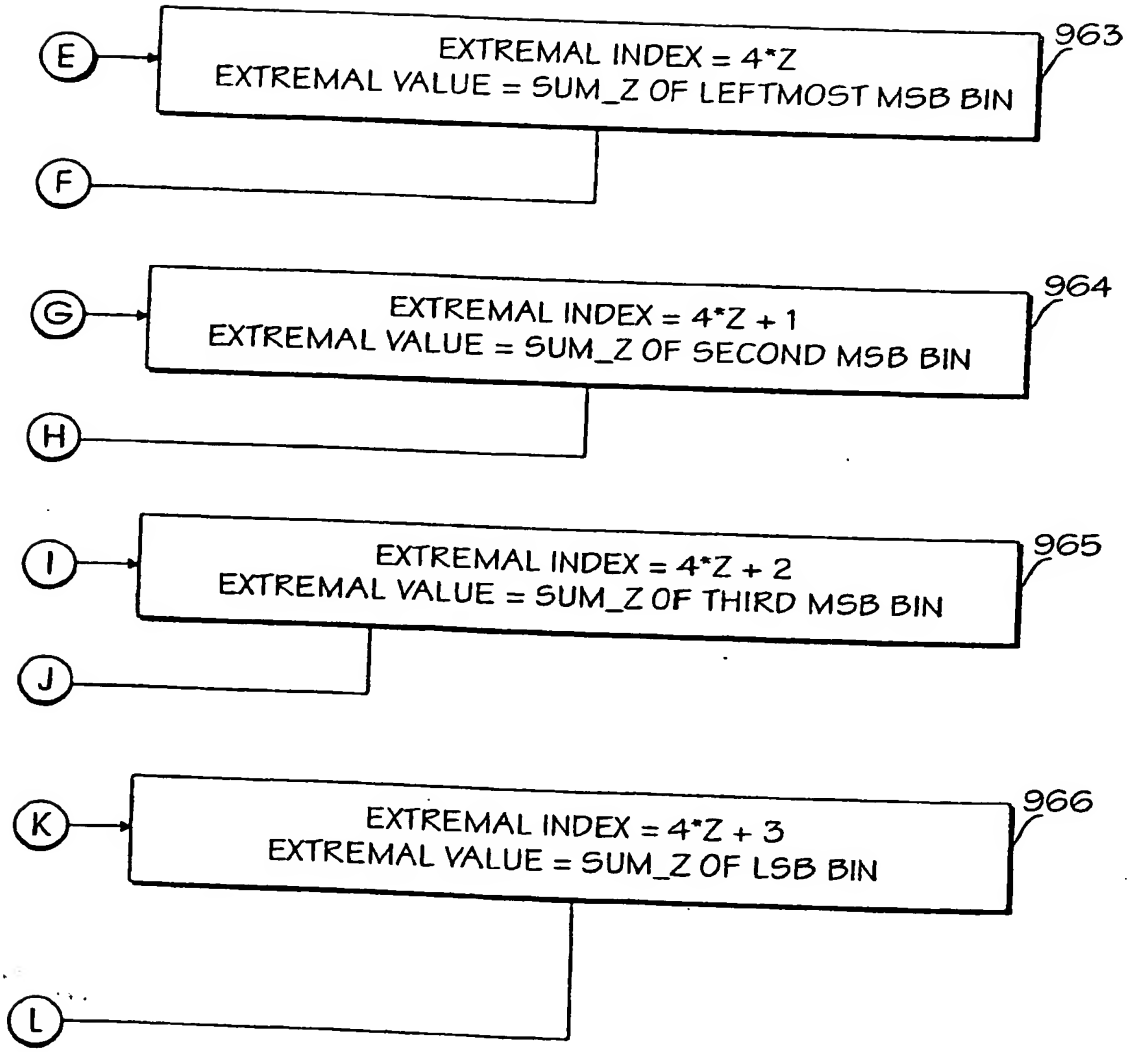


FIG. 42(D)

20120230004

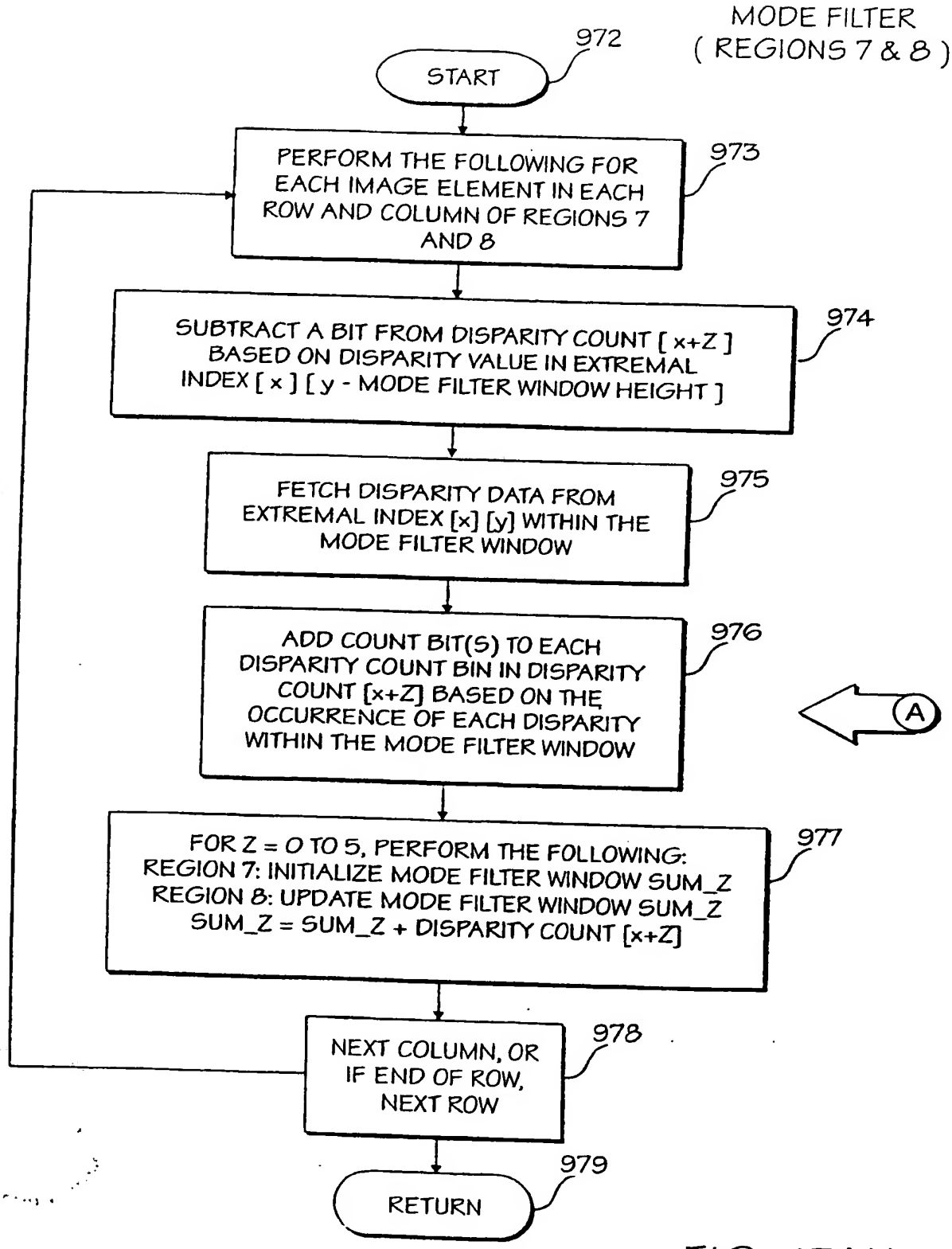


FIG. 43(A)

MODE FILTER
(REGIONS 7 & 8)

980

DISP	DISPARITY COUNT [x+Z]	
0	[x]	**00** 00 00 00
1	[x]	00 **00** 00 00
2	[x]	00 00 **00** 00
3	[x]	00 00 00 **00**
4	[x+1]	**00** 00 00 00
5	[x+1]	00 **00** 00 00
6	[x+1]	00 00 **00** 00
7	[x+1]	00 00 00 **00**
8	[x+2]	**00** 00 00 00
9	[x+2]	00 **00** 00 00
10	[x+2]	00 00 **00** 00
11	[x+2]	00 00 00 **00**
12	[x+3]	**00** 00 00 00
13	[x+3]	00 **00** 00 00
14	[x+3]	00 00 **00** 00
15	[x+3]	00 00 00 **00**
16	[x+4]	**00** 00 00 00
17	[x+4]	00 **00** 00 00
18	[x+4]	00 00 **00** 00
19	[x+4]	00 00 00 **00**
20	[x+5]	**00** 00 00 00
21	[x+5]	00 **00** 00 00
22	[x+5]	00 00 **00** 00
23	[x+5]	00 00 00 **00**

A

FIG. 43(B)

EXHIBIT 2080

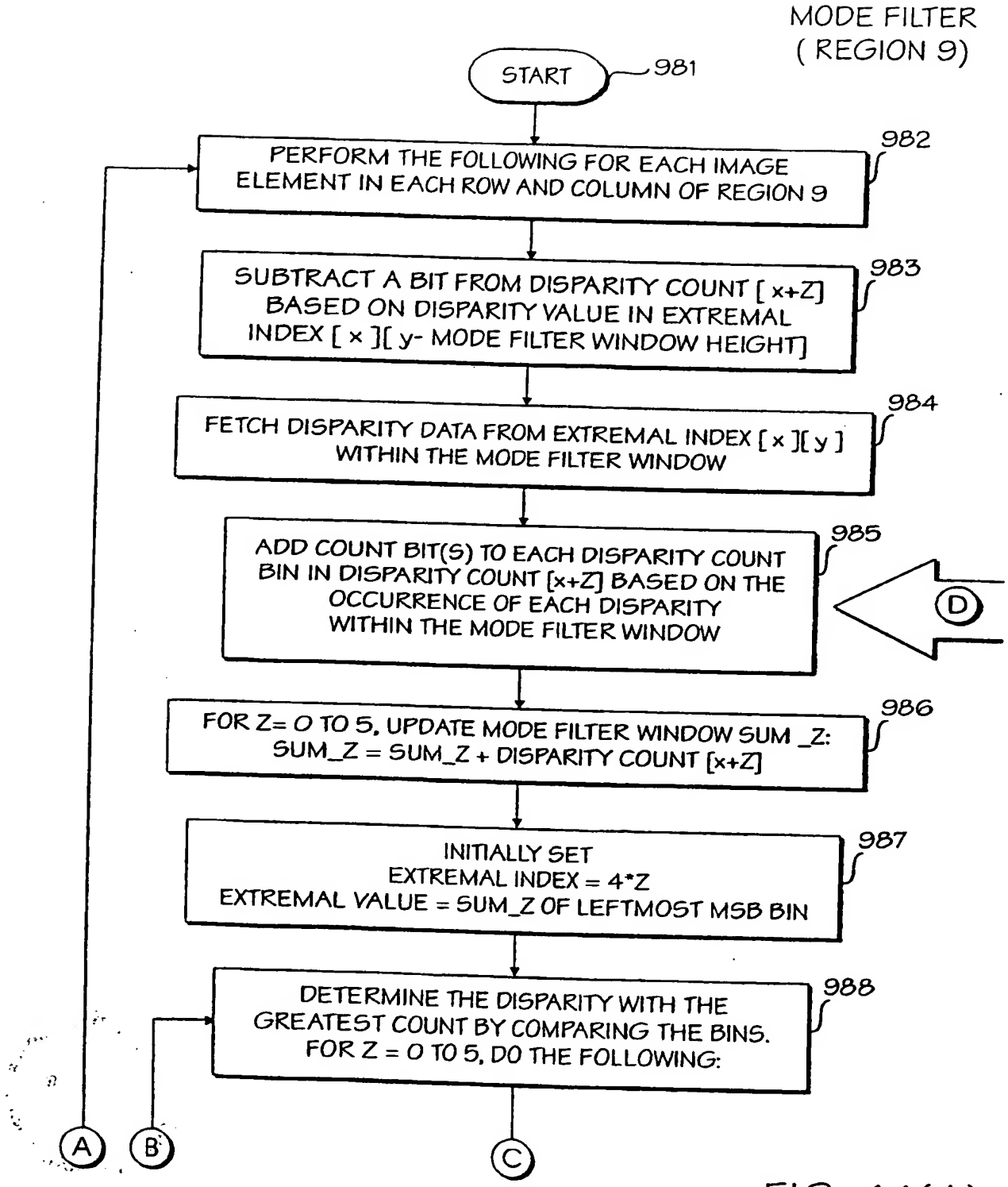


FIG. 44(A)

MODE FILTER
(REGION 9)

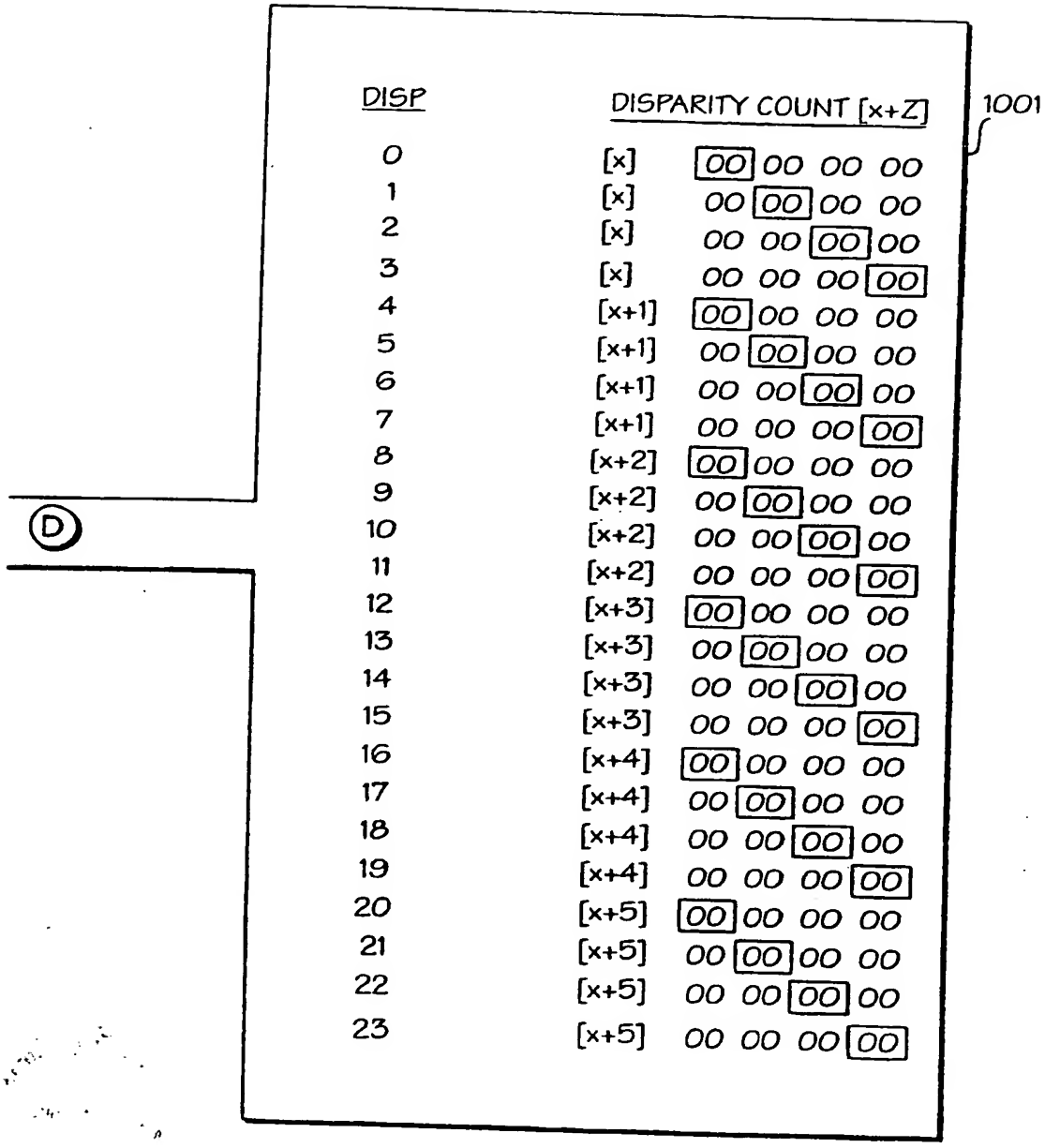


FIG. 44(B)

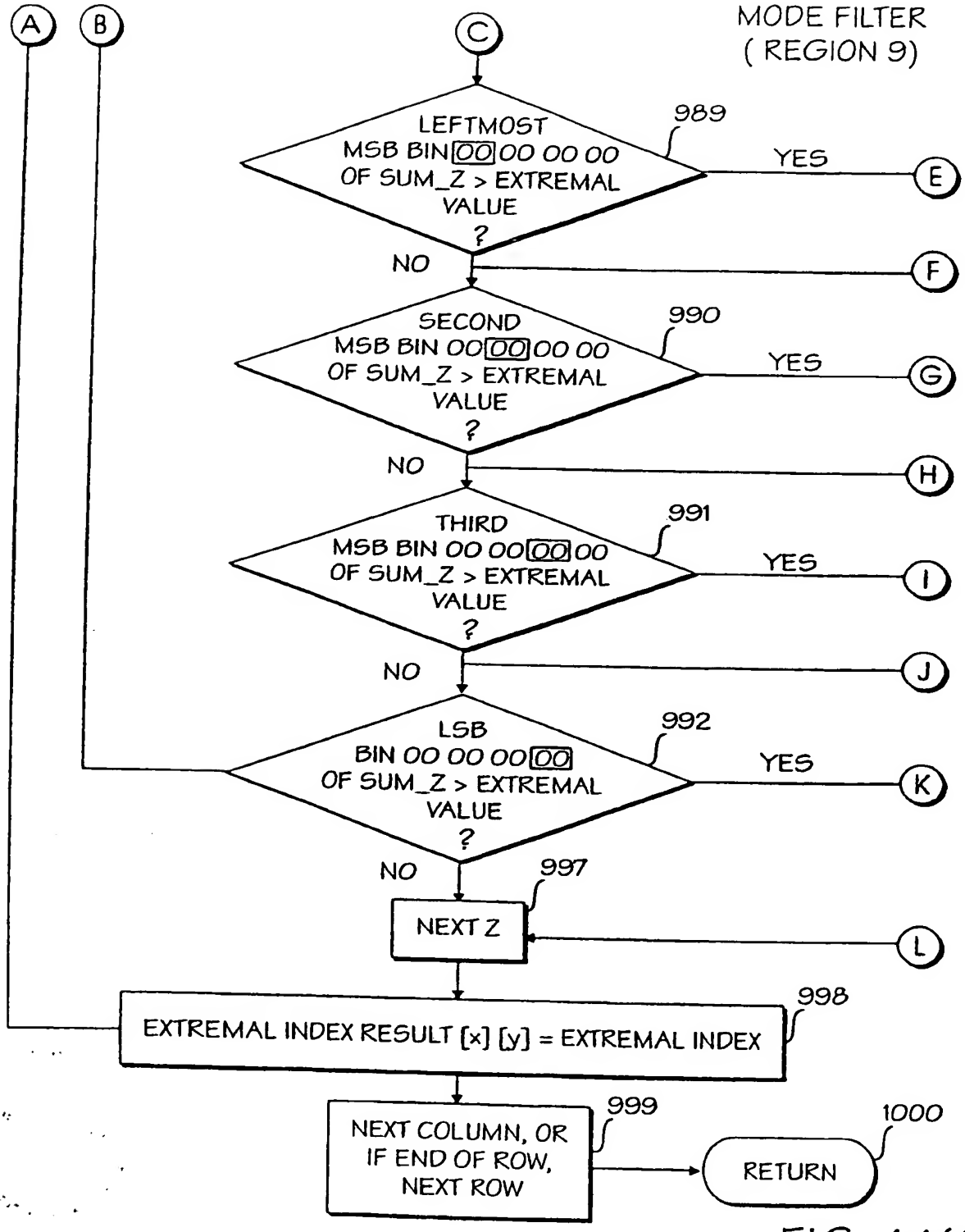

MODE FILTER
(REGION 9)
A
B
C
LEFTMOST MSB BIN OO OO OO OO OF SUM_Z > EXTREMAL VALUE ?
989
YES
E
NO
F
SECOND MSB BIN OO OO OO OO OF SUM_Z > EXTREMAL VALUE ?
990
YES
G
NO
H
THIRD MSB BIN OO OO OO OO OF SUM_Z > EXTREMAL VALUE ?
991
YES
I
NO
J
LSB BIN OO OO OO OO OF SUM_Z > EXTREMAL VALUE ?
992
YES
K
NO
997
NEXT Z
L
EXTREMAL INDEX RESULT [x] [y] = EXTREMAL INDEX
998
NEXT COLUMN, OR IF END OF ROW, NEXT ROW
999
RETURN
1000

FIG. 44(C)

MODE FILTER
(REGION 9)

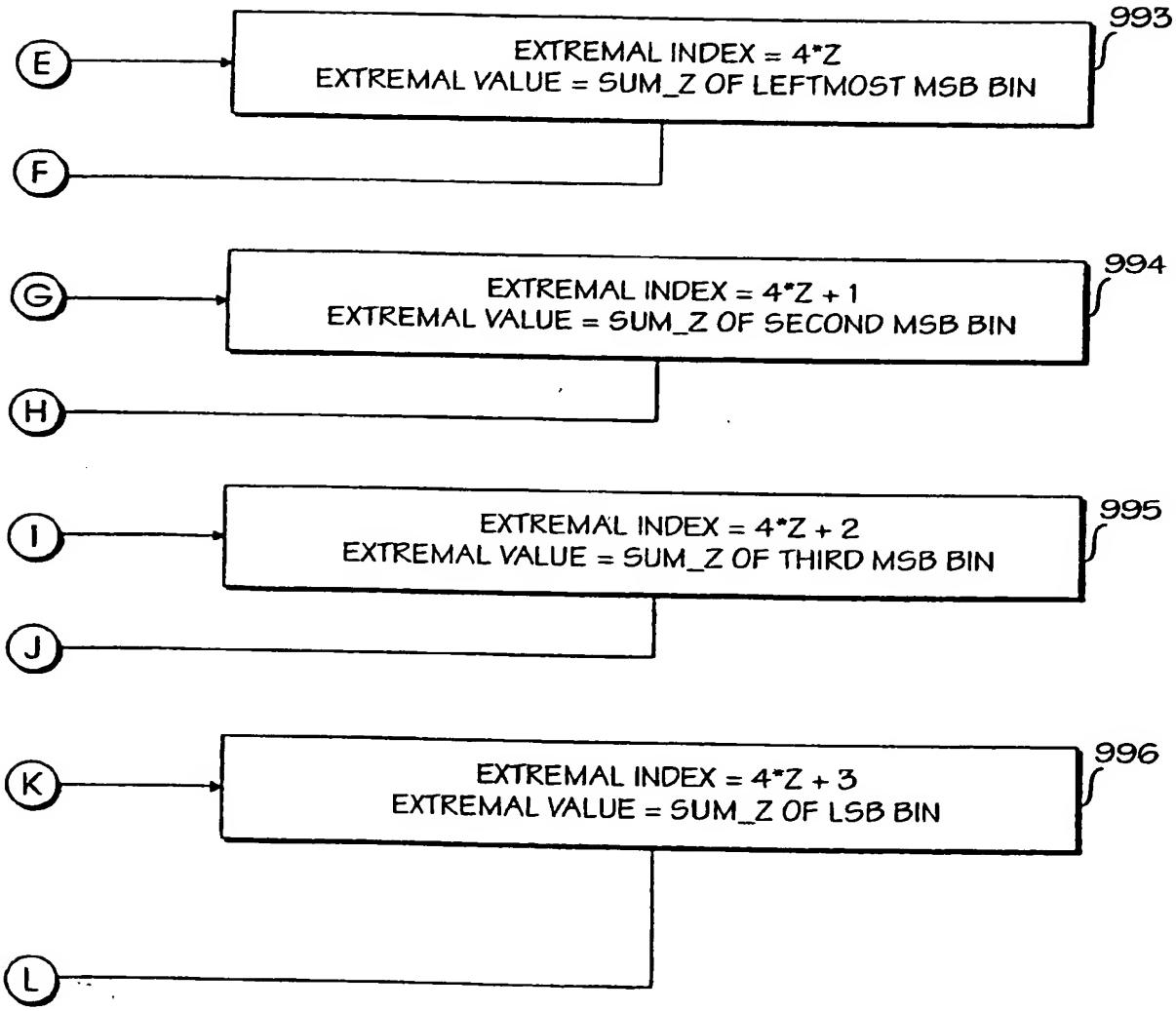


FIG. 44(D)

20142650 2006001

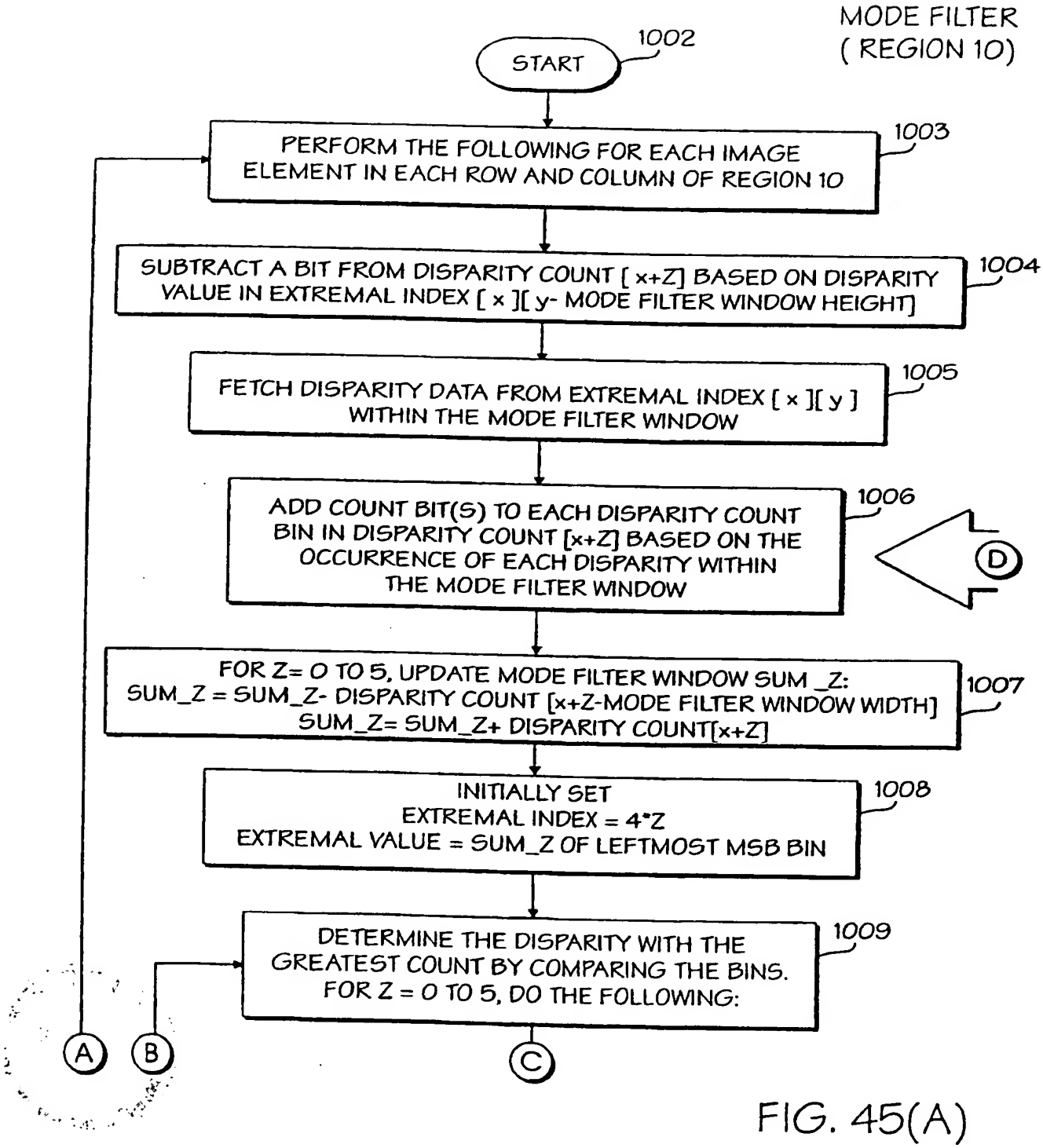


FIG. 45(A)

MODE FILTER
(REGION 10)

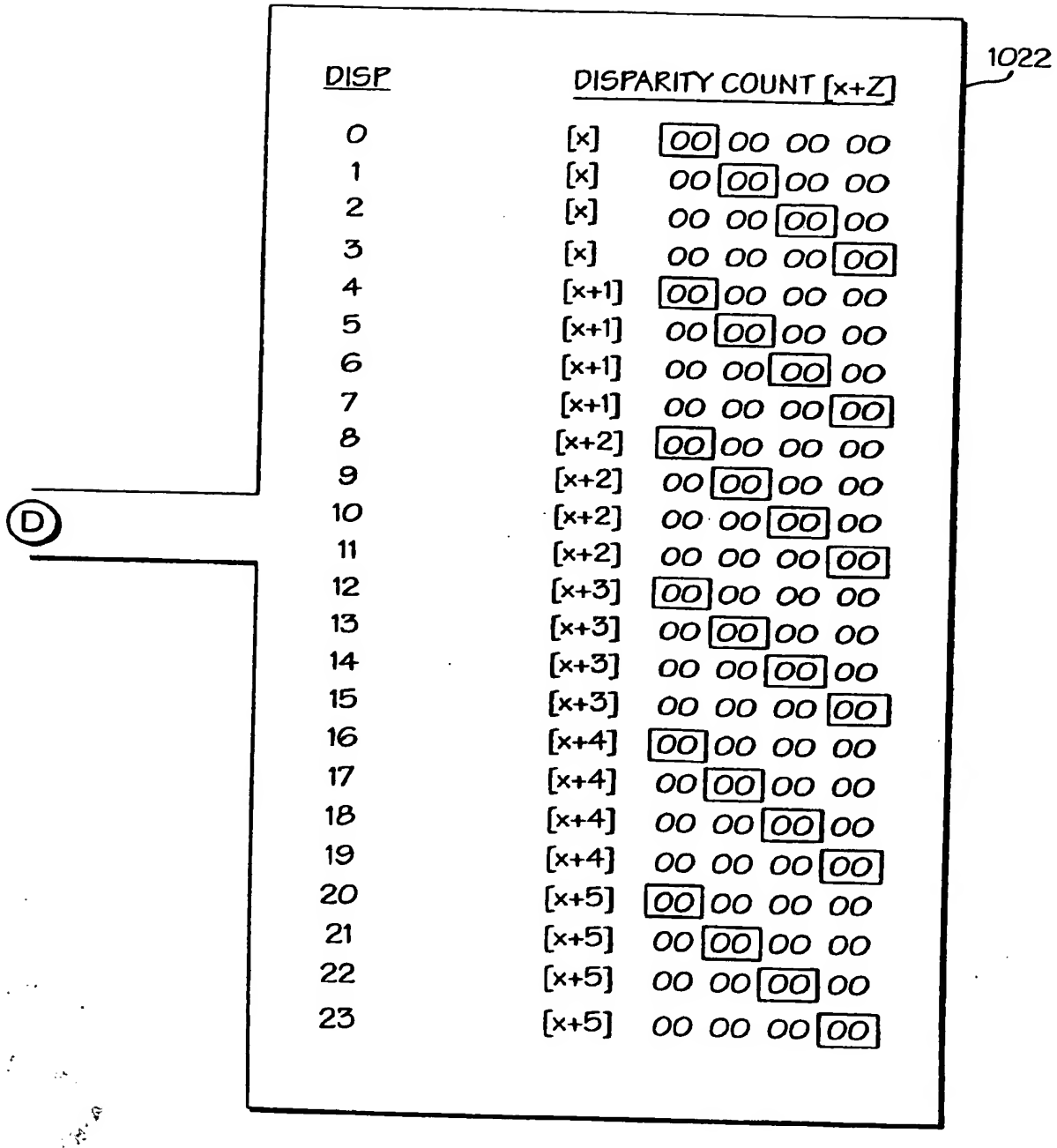


FIG. 45(B)

09/09/2004

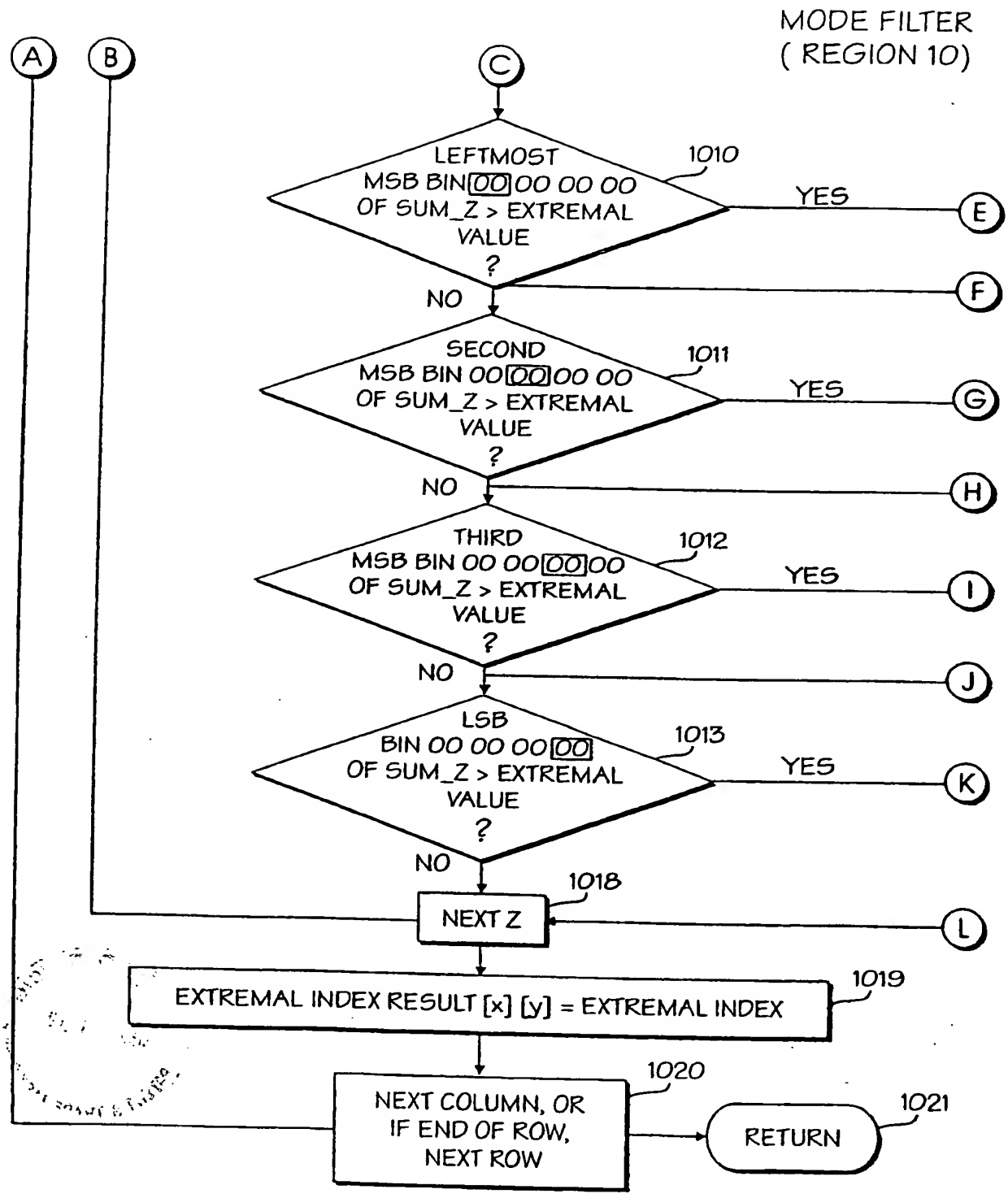


FIG. 45(C)

MODE FILTER
(REGION 10)

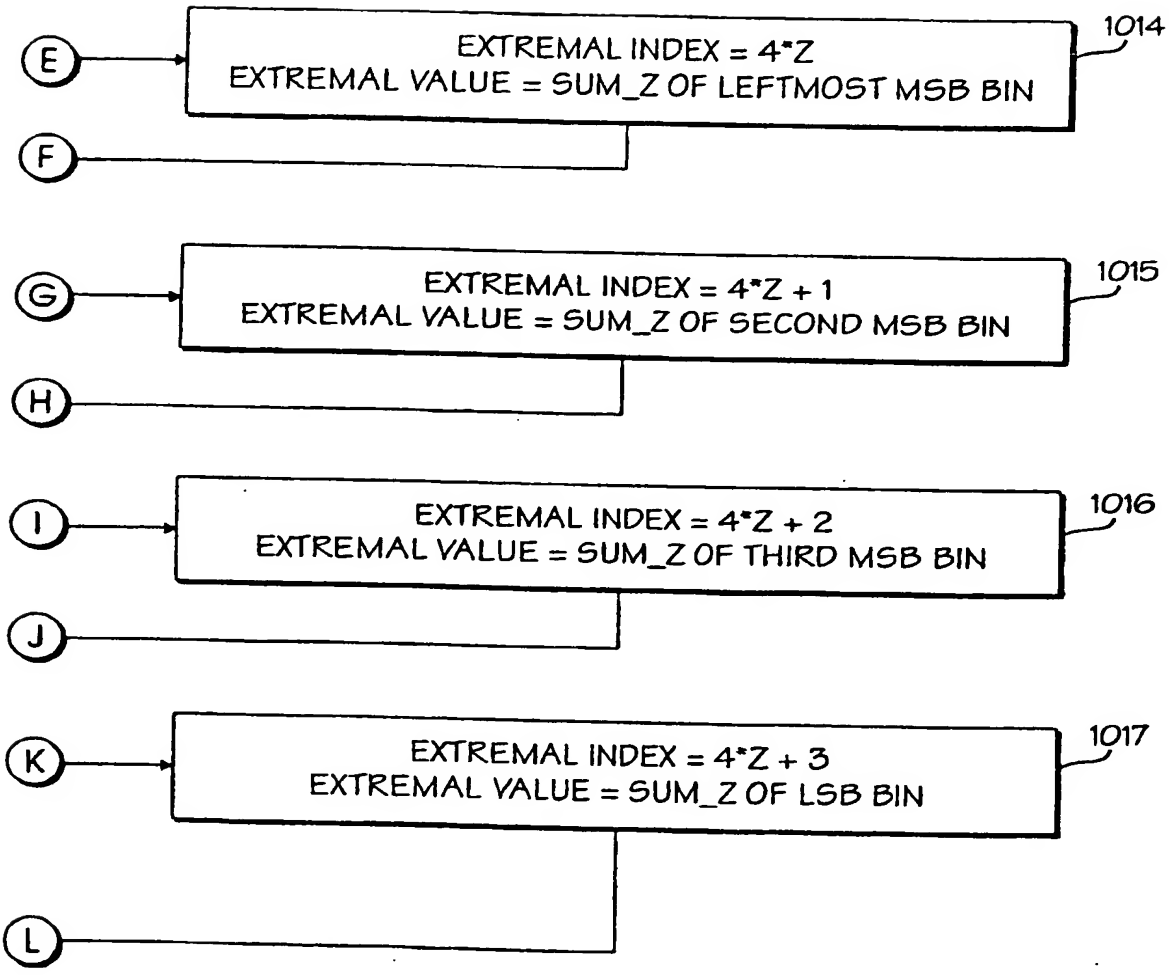


FIG. 45(D)

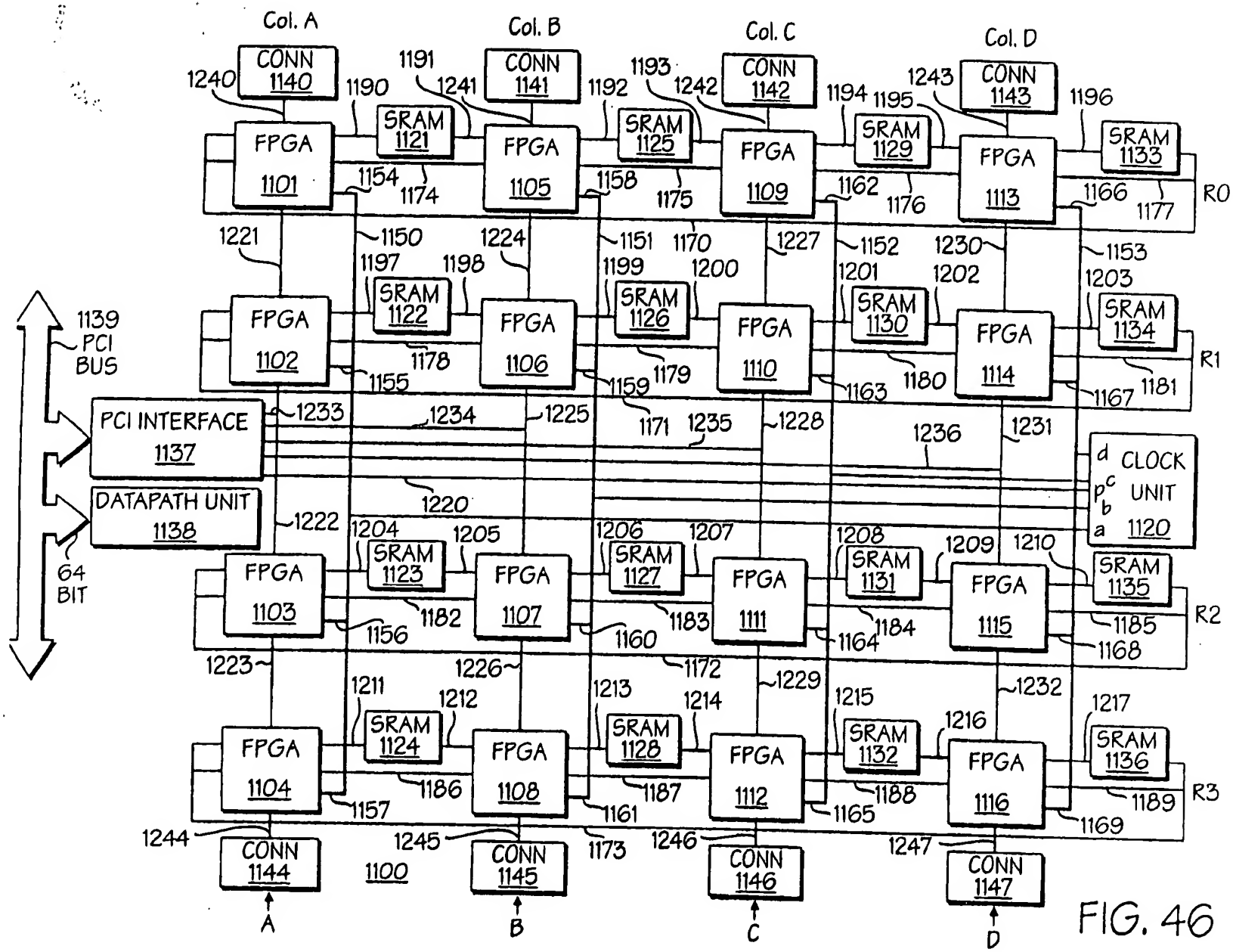

Col. A
Col. B
Col. C
Col. D
CONN 1140
CONN 1141
CONN 1142
CONN 1143
SRAM 1121
SRAM 1125
SRAM 1129
SRAM 1133
FPGA 1101
FPGA 1105
FPGA 1109
FPGA 1113
R0
SRAM 1122
SRAM 1126
SRAM 1130
SRAM 1134
FPGA 1102
FPGA 1106
FPGA 1110
FPGA 1114
R1
1139 PCI BUS
PCI INTERFACE 1137
DATAPATH UNIT 1138
64 BIT
CLOCK UNIT 1120
SRAM 1123
SRAM 1127
SRAM 1131
SRAM 1135
FPGA 1103
FPGA 1107
FPGA 1111
FPGA 1115
R2
SRAM 1124
SRAM 1128
SRAM 1132
SRAM 1136
FPGA 1104
FPGA 1108
FPGA 1112
FPGA 1116
R3
CONN 1144
CONN 1145
CONN 1146
CONN 1147
1100
A
B
C
D

FIG. 46

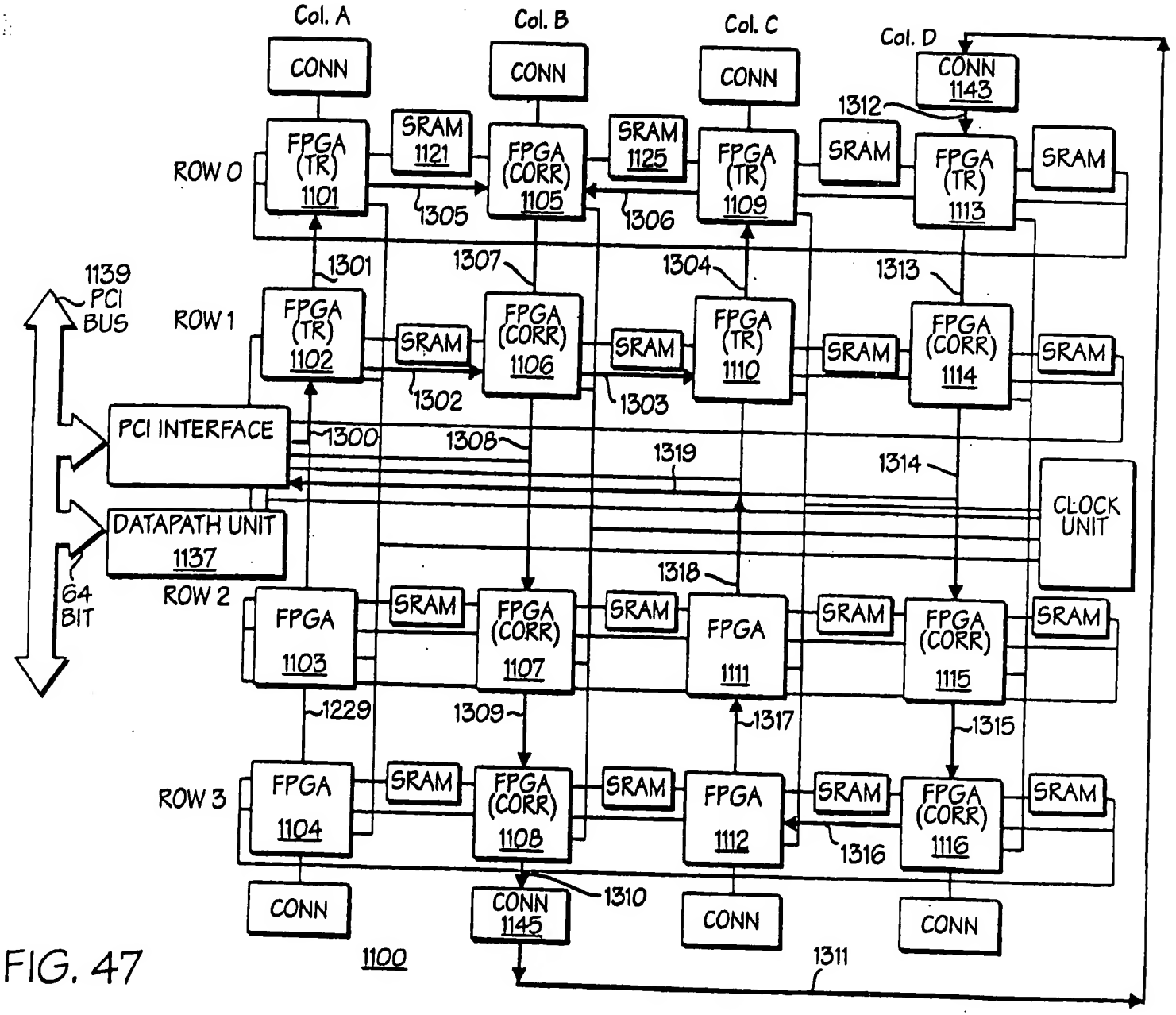

Col. A
Col. B
Col. C
Col. D
CONN
CONN
CONN
CONN 1143
1312
ROW 0
FPGA (TR) 1101
SRAM 1121
FPGA (CORR) 1105
SRAM 1125
FPGA (TR) 1109
SRAM
FPGA (TR) 1113
SRAM
1305
1306
1139 PCI BUS
1301
1307
1304
1313
ROW 1
FPGA (TR) 1102
SRAM
FPGA (CORR) 1106
SRAM
FPGA (TR) 1110
SRAM
FPGA (CORR) 1114
SRAM
1302
1303
PCI INTERFACE
1300
1308
1319
1314
CLOCK UNIT
DATAPATH UNIT 1137
64 BIT
1318
ROW 2
FPGA 1103
SRAM
FPGA (CORR) 1107
SRAM
FPGA 1111
SRAM
FPGA (CORR) 1115
SRAM
1229
1309
1317
1315
ROW 3
FPGA 1104
SRAM
FPGA (CORR) 1108
SRAM
FPGA 1112
SRAM
FPGA (CORR) 1116
SRAM
1316
1310
CONN
CONN 1145
CONN
CONN
1100
1311

FIG. 47

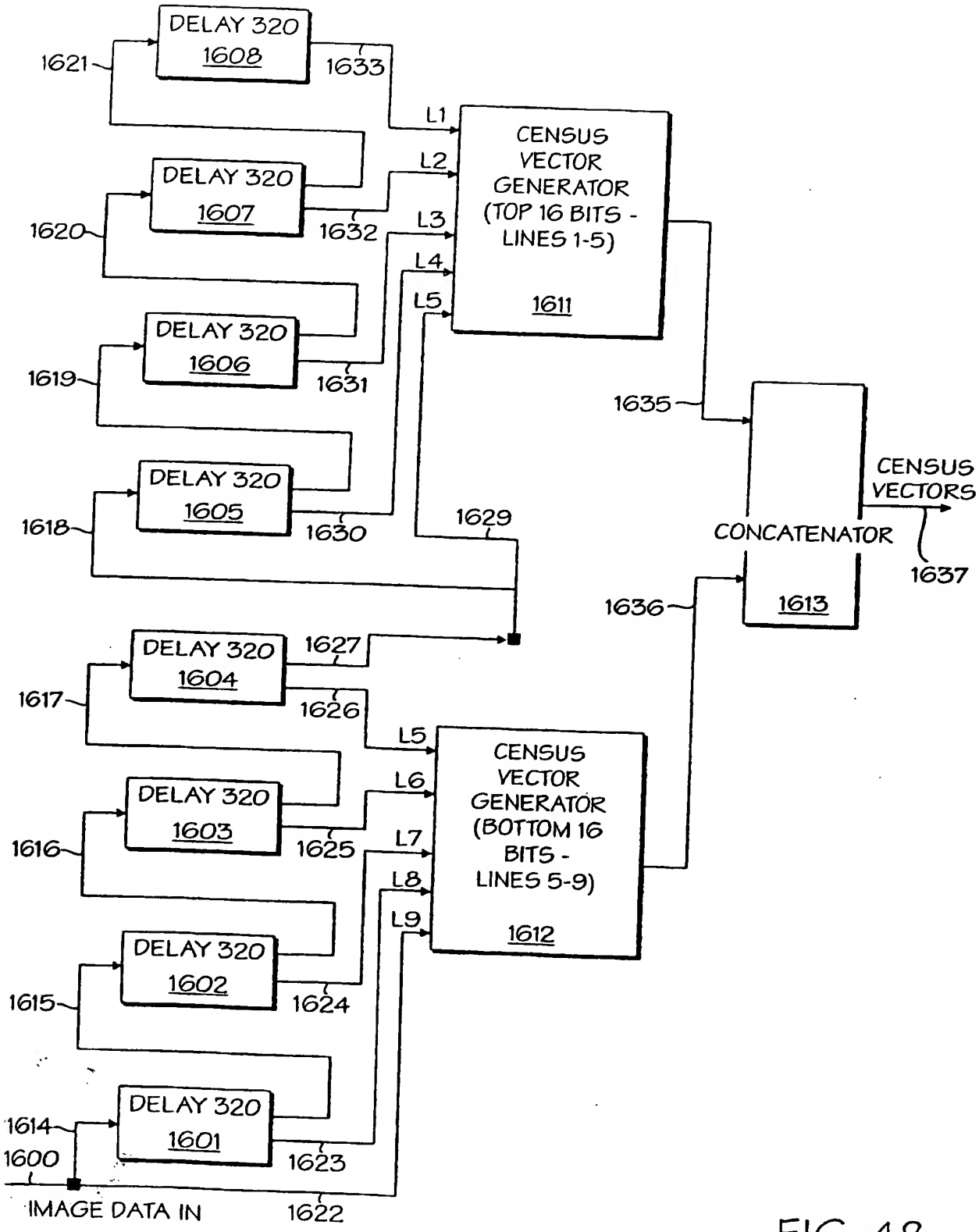

DELAY 320
1608
1621
1633
L1
CENSUS
VECTOR
GENERATOR
(TOP 16 BITS -
LINES 1-5)
1611
DELAY 320
1607
1620
1632
L2
L3
L4
L5
DELAY 320
1606
1619
1631
1635
DELAY 320
1605
1618
1630
1629
CENSUS
VECTORS
CONCATENATOR
1613
1637
1636
DELAY 320
1604
1617
1627
1626
L5
CENSUS
VECTOR
GENERATOR
(BOTTOM 16
BITS -
LINES 5-9)
1612
DELAY 320
1603
1616
1625
L6
L7
L8
L9
DELAY 320
1602
1615
1624
DELAY 320
1601
1614
1623
1600
IMAGE DATA IN
1622

FIG. 48

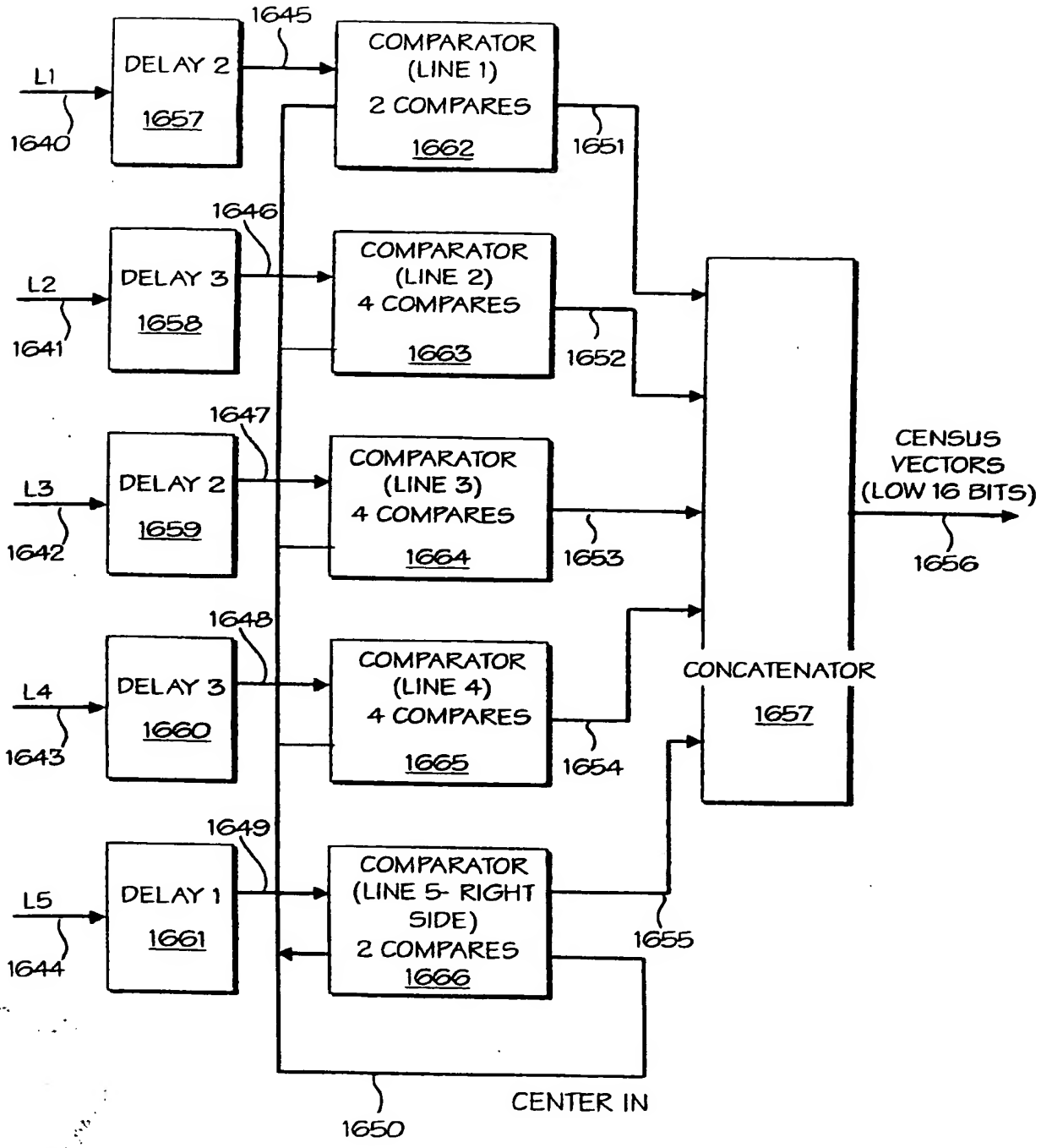

L1
1640
DELAY 2
1657
1645
COMPARATOR
(LINE 1)
2 COMPARES
1662
1651
L2
1641
DELAY 3
1658
1646
COMPARATOR
(LINE 2)
4 COMPARES
1663
1652
L3
1642
DELAY 2
1659
1647
COMPARATOR
(LINE 3)
4 COMPARES
1664
1653
L4
1643
DELAY 3
1660
1648
COMPARATOR
(LINE 4)
4 COMPARES
1665
1654
L5
1644
DELAY 1
1661
1649
COMPARATOR
(LINE 5- RIGHT
SIDE)
2 COMPARES
1666
1655
CONCATENATOR
1657
CENSUS
VECTORS
(LOW 16 BITS)
1656
CENTER IN
1650

FIG. 49

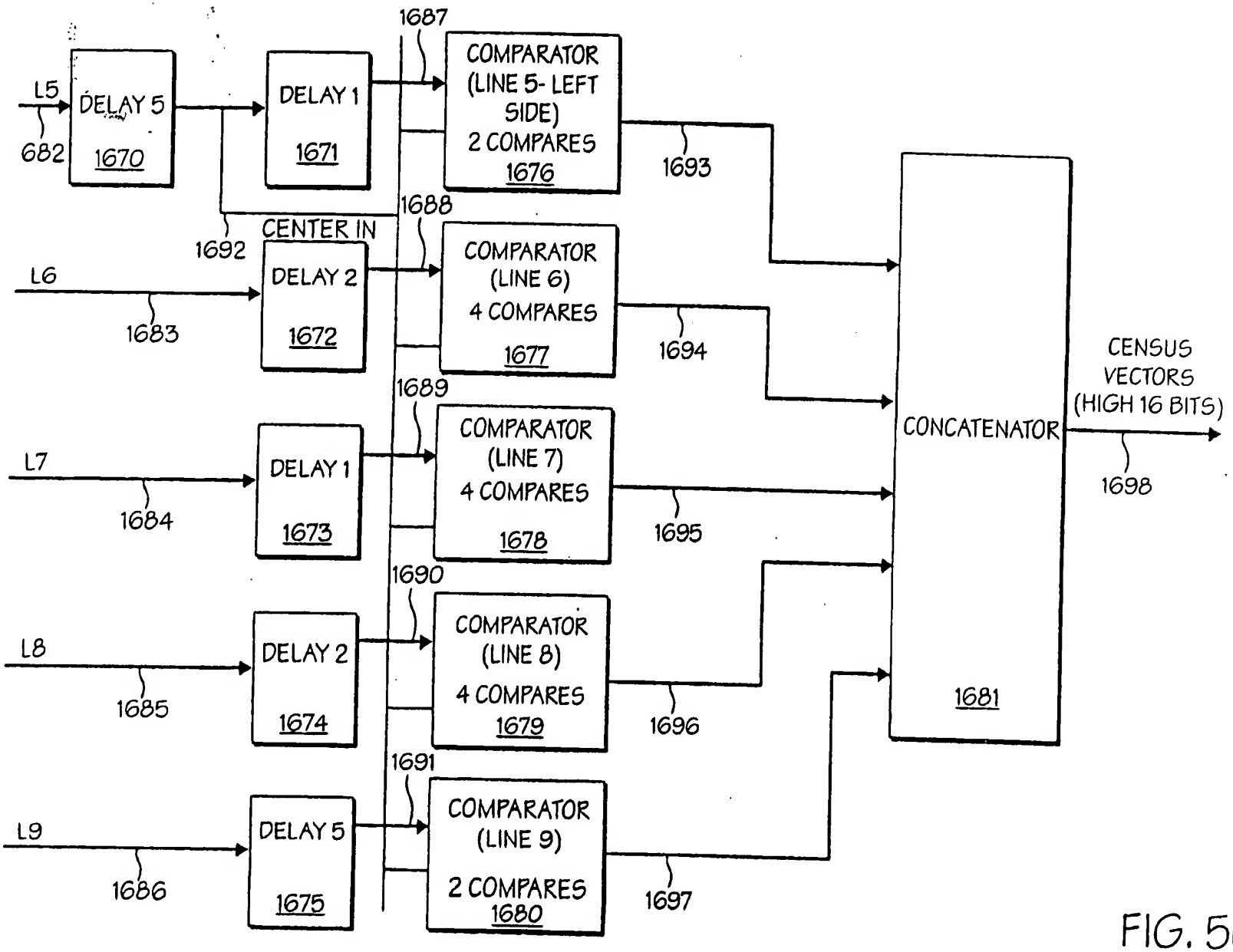

L5
682
DELAY 5
1670
DELAY 1
1671
1687
COMPARATOR
(LINE 5- LEFT
SIDE)
2 COMPARES
1676
1693
1692
CENTER IN
1688
L6
1683
DELAY 2
1672
COMPARATOR
(LINE 6)
4 COMPARES
1677
1694
1689
L7
1684
DELAY 1
1673
COMPARATOR
(LINE 7)
4 COMPARES
1678
1695
1690
L8
1685
DELAY 2
1674
COMPARATOR
(LINE 8)
4 COMPARES
1679
1696
1691
L9
1686
DELAY 5
1675
COMPARATOR
(LINE 9)
2 COMPARES
1680
1697
CONCATENATOR
1681
CENSUS
VECTORS
(HIGH 16 BITS)
1698

FIG. 50

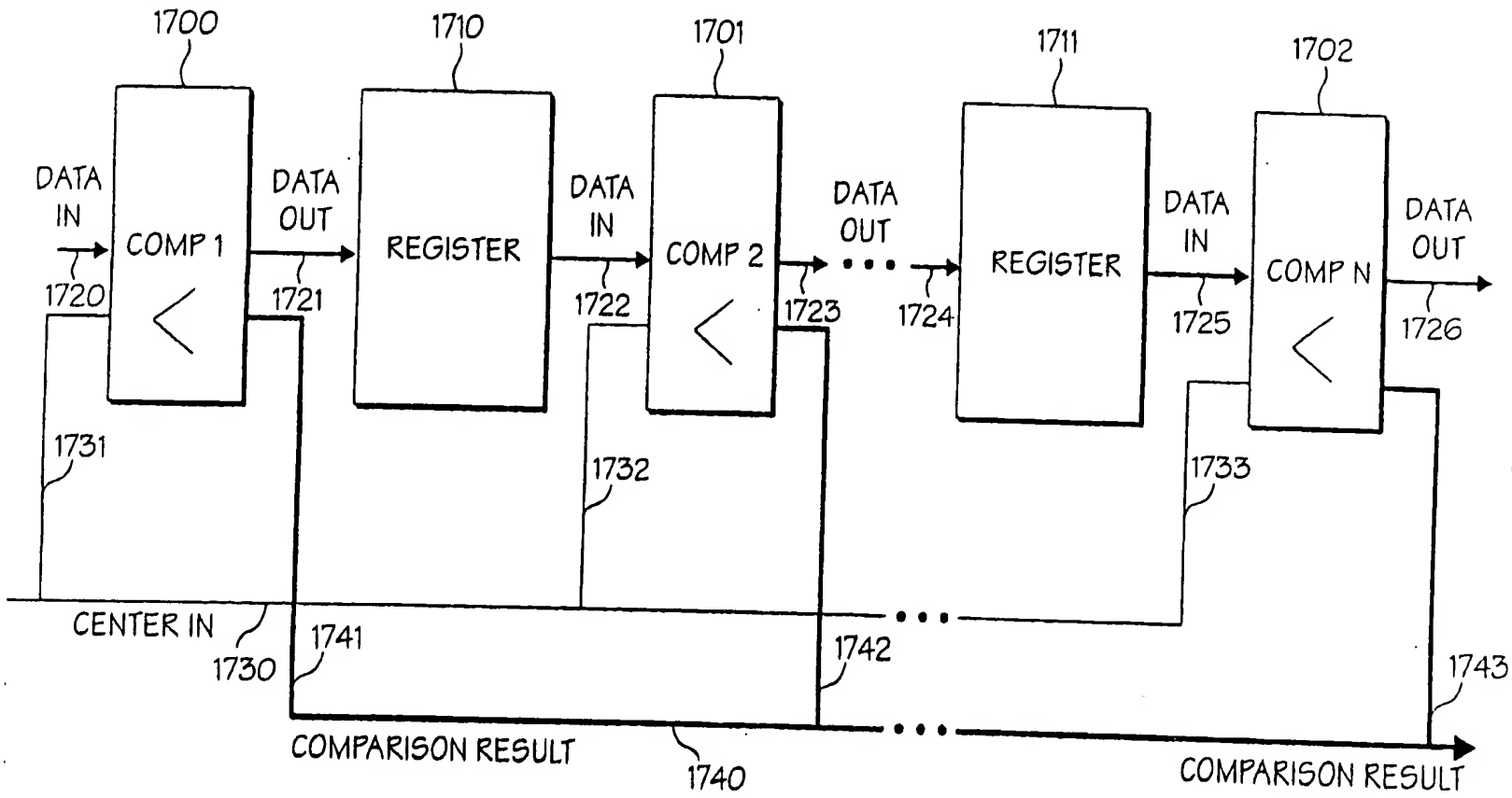

1700
1710
1701
1711
1702
DATA IN
COMP 1
DATA OUT
REGISTER
DATA IN
COMP 2
DATA OUT
REGISTER
DATA IN
COMP N
DATA OUT
1720
1721
1722
1723
1724
1725
1726
1731
1732
1733
CENTER IN
1730
1741
1742
1743
COMPARISON RESULT
1740
COMPARISON RESULT

FIG. 51

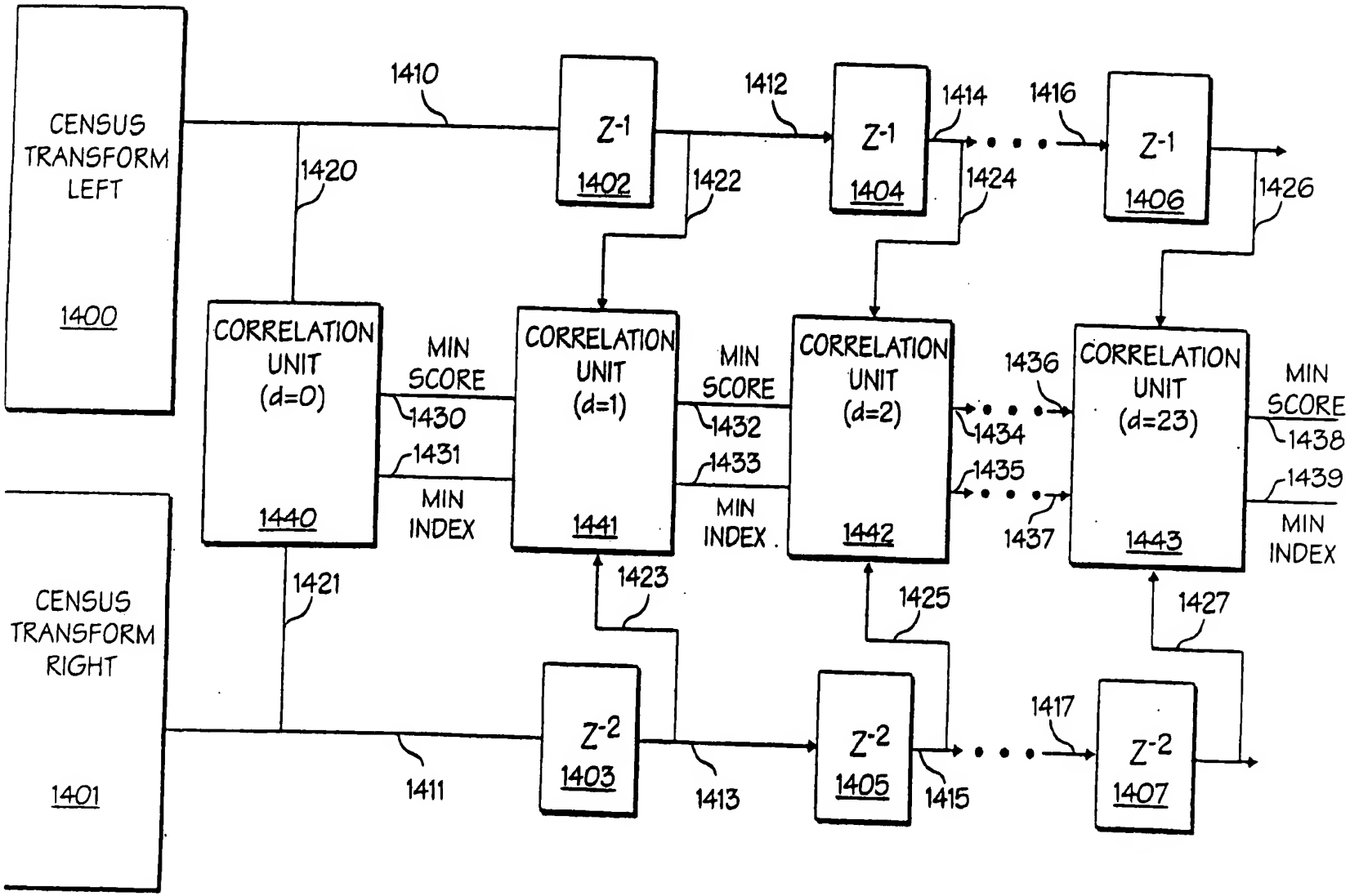

CENSUS TRANSFORM LEFT
1400
CENSUS TRANSFORM RIGHT
1401
1410
1412
1414
1416
Z-1
1402
Z-1
1404
Z-1
1406
1420
1422
1424
1426
CORRELATION UNIT (d=0)
1440
CORRELATION UNIT (d=1)
1441
CORRELATION UNIT (d=2)
1442
CORRELATION UNIT (d=23)
1443
MIN SCORE
1430
MIN INDEX
1431
MIN SCORE
1432
MIN INDEX
1433
1434
1435
1436
1437
MIN SCORE
1438
MIN INDEX
1439
1421
1423
1425
1427
Z-2
1403
Z-2
1405
Z-2
1407
1411
1413
1415
1417

Fig. 52

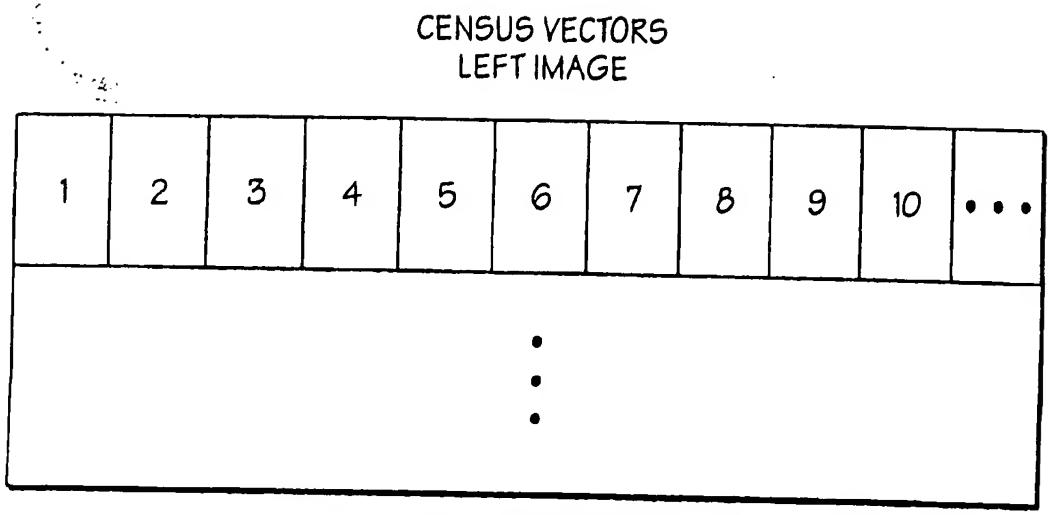


Fig. 53(A)

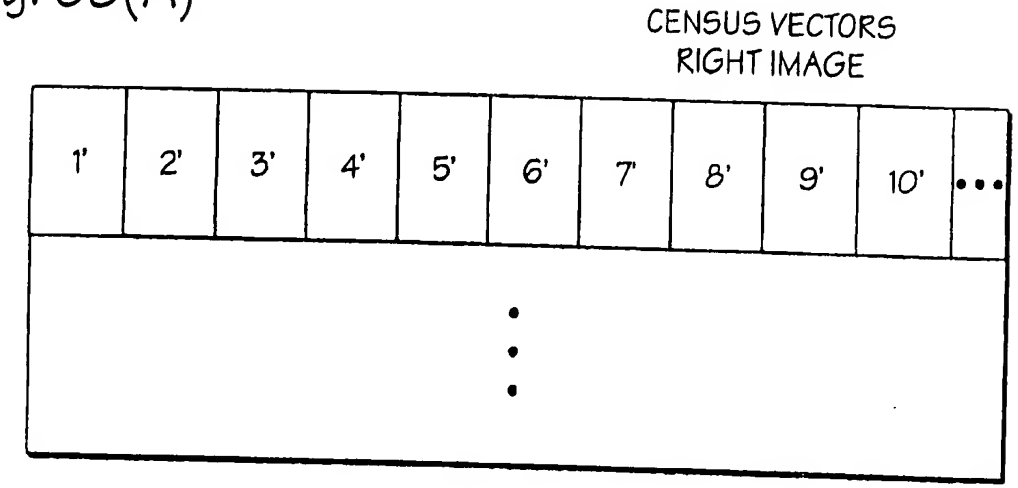


Fig. 53(B)

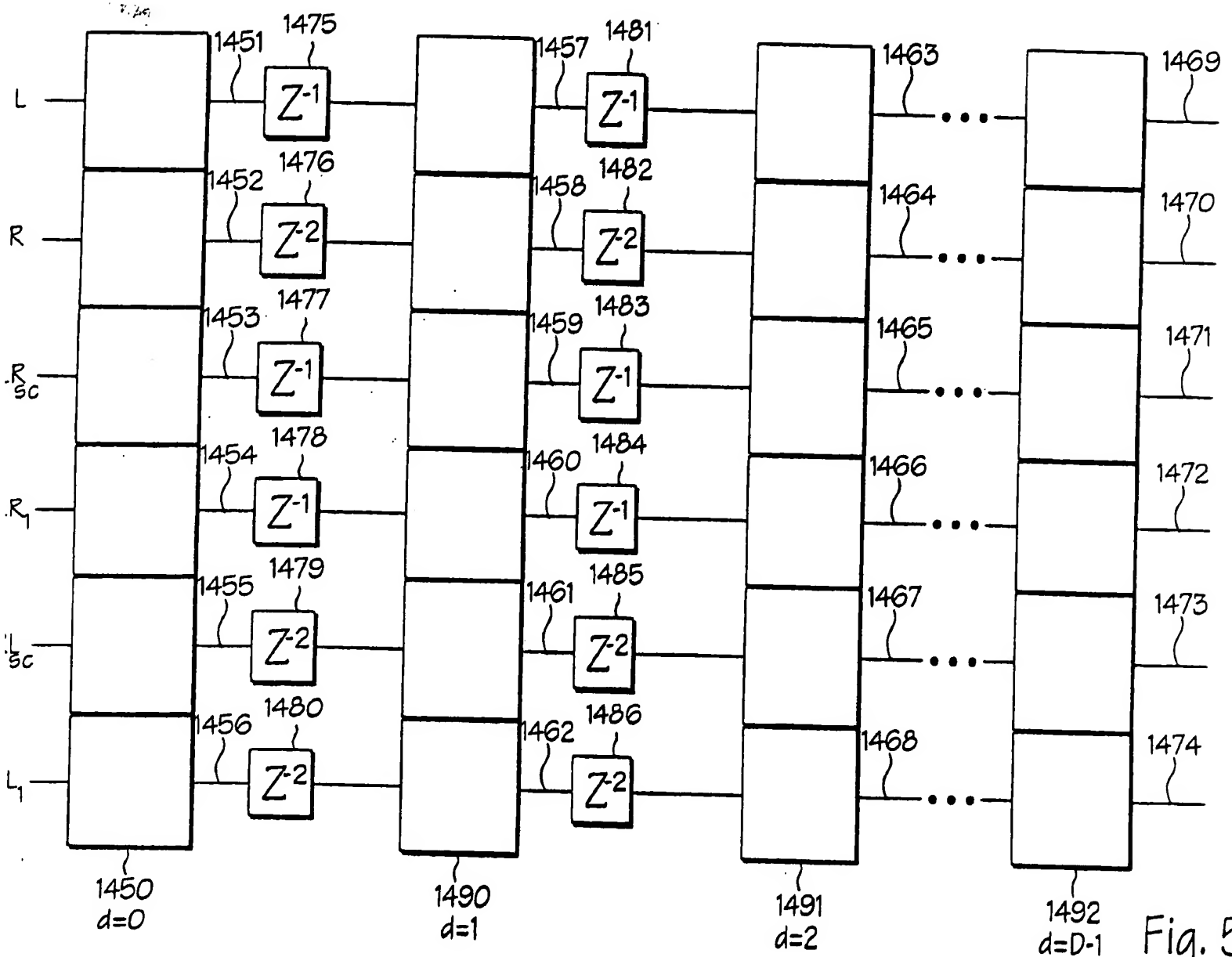

L
R
R_{SC}
R_1
L_{SC}
L_1
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
Z^{-1}
Z^{-2}
1450
d=0
1490
d=1
1491
d=2
1492
d=D-1

Fig. 54

15 IMAGE ELEMENTS (1 TO 15 FOR L; 1' TO 15' FOR R)
D=5 (d= {0, 1, 2, 3, 4})

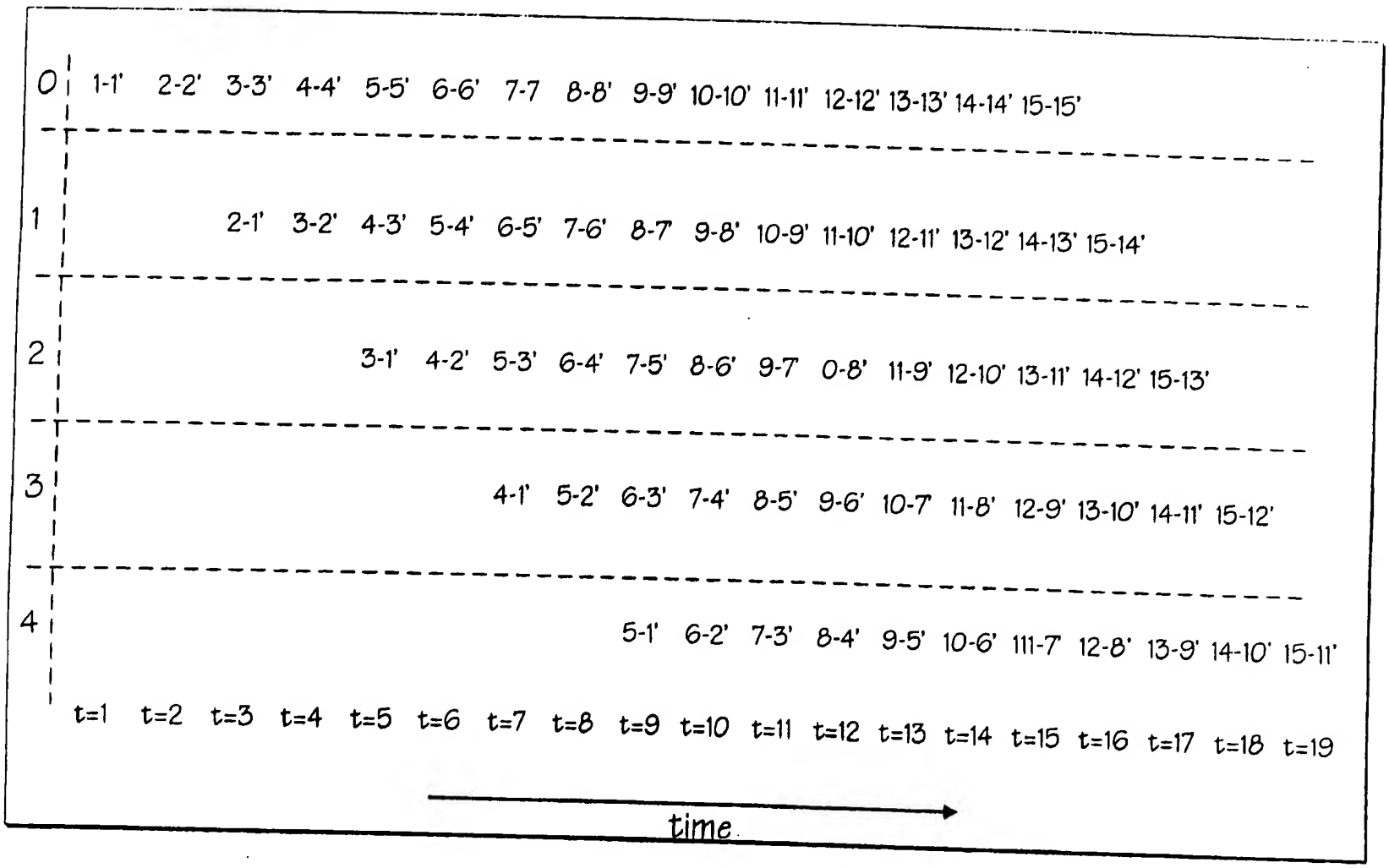


FIG. 55

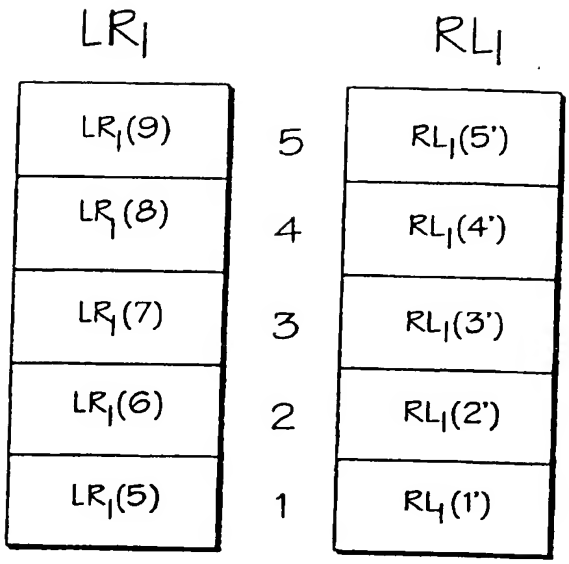


Fig. 56(A)

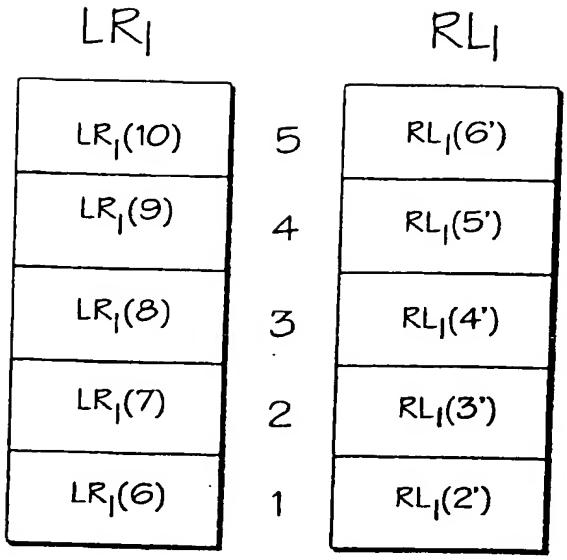


Fig. 56(B)

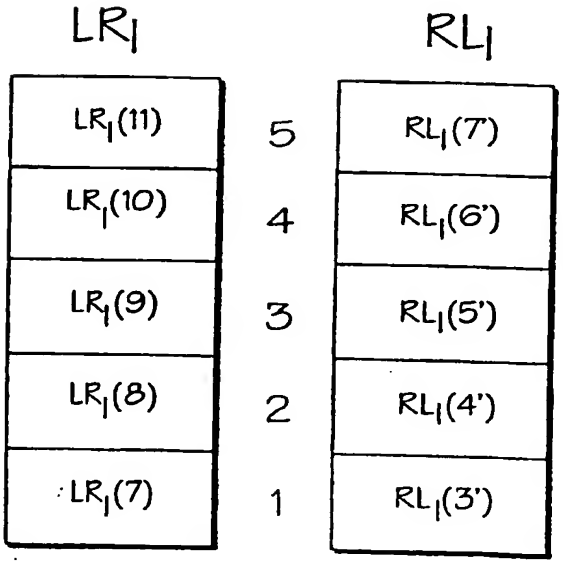


Fig. 56(C)

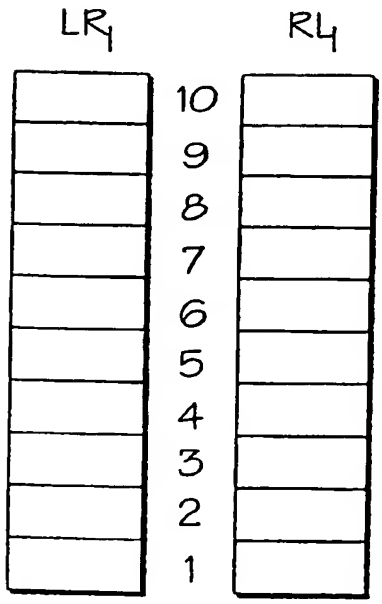


Fig. 56(D)

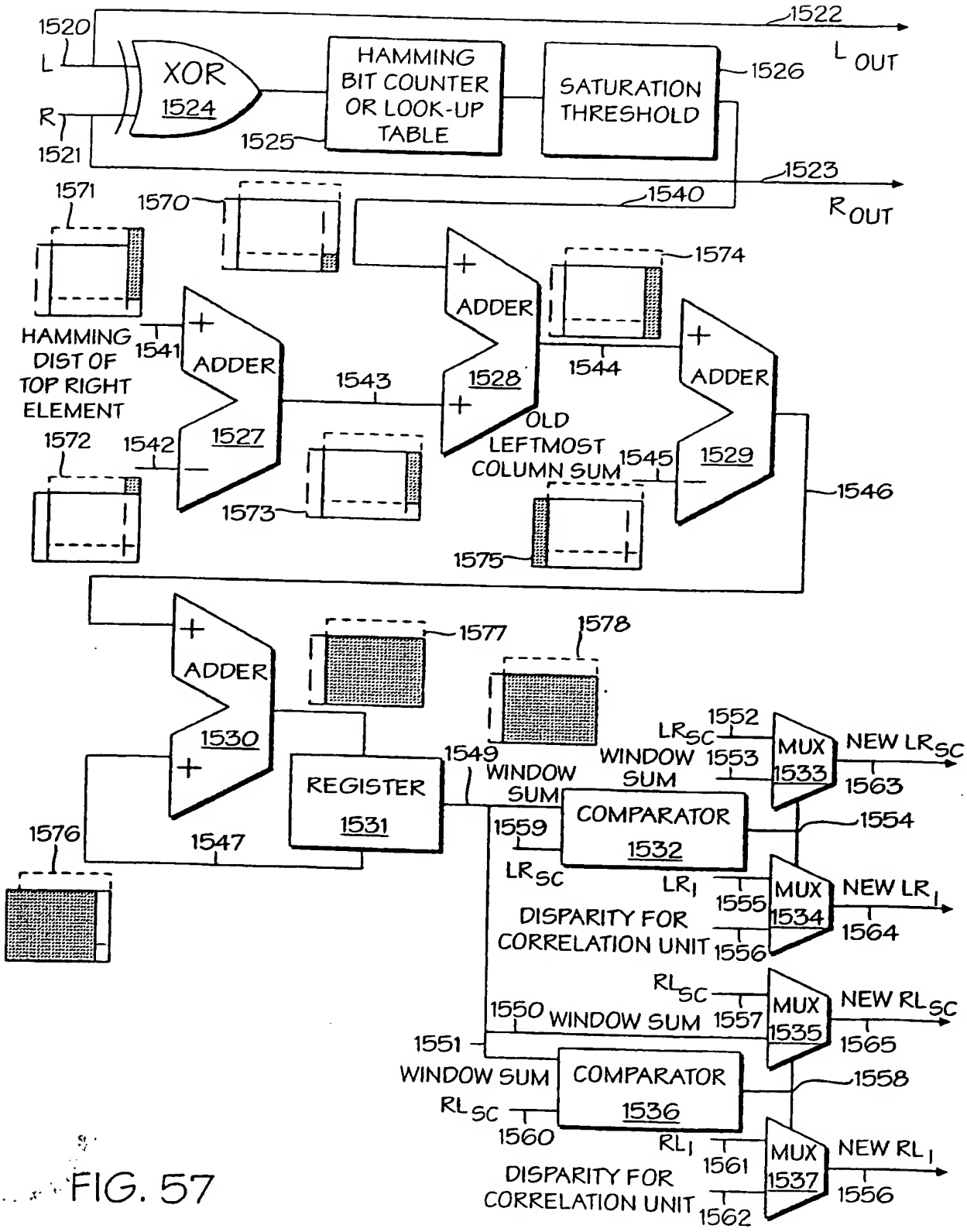

1520
L
R
1521
XOR
1524
1525
HAMMING BIT COUNTER OR LOOK-UP TABLE
SATURATION THRESHOLD
1526
1522
L OUT
1523
R OUT
1540
1571
1570
HAMMING DIST OF TOP RIGHT ELEMENT
1541
ADDER
1527
1542
1572
1573
1543
ADDER
1528
1574
1544
OLD LEFTMOST COLUMN SUM
1545
ADDER
1529
1546
1575
ADDER
1530
1577
1578
REGISTER
1531
1547
1576
1549
WINDOW SUM
1552
LRSC
WINDOW SUM
1553
MUX
1533
NEW LRSC
1563
COMPARATOR
1532
1554
1559
LRSC
LRI
1555
MUX
1534
NEW LRI
1564
DISPARITY FOR CORRELATION UNIT
1556
RLSC
1550
WINDOW SUM
1557
MUX
1535
NEW RLSC
1565
1551
WINDOW SUM
COMPARATOR
1536
1558
RLSC
1560
RLI
1561
MUX
1537
NEW RLI
1566
DISPARITY FOR CORRELATION UNIT
1562

FIG. 57

20120238007

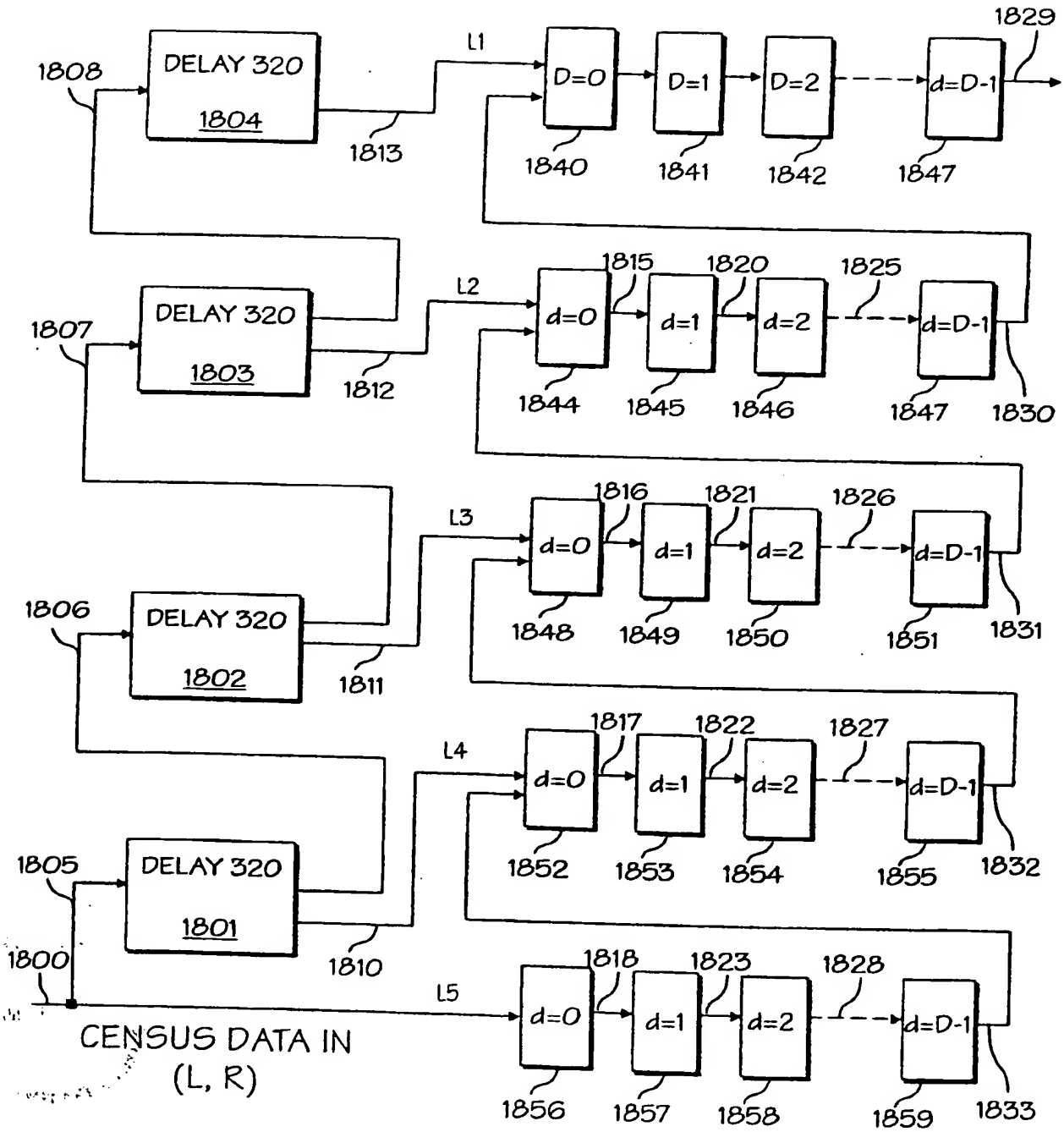


FIG. 58

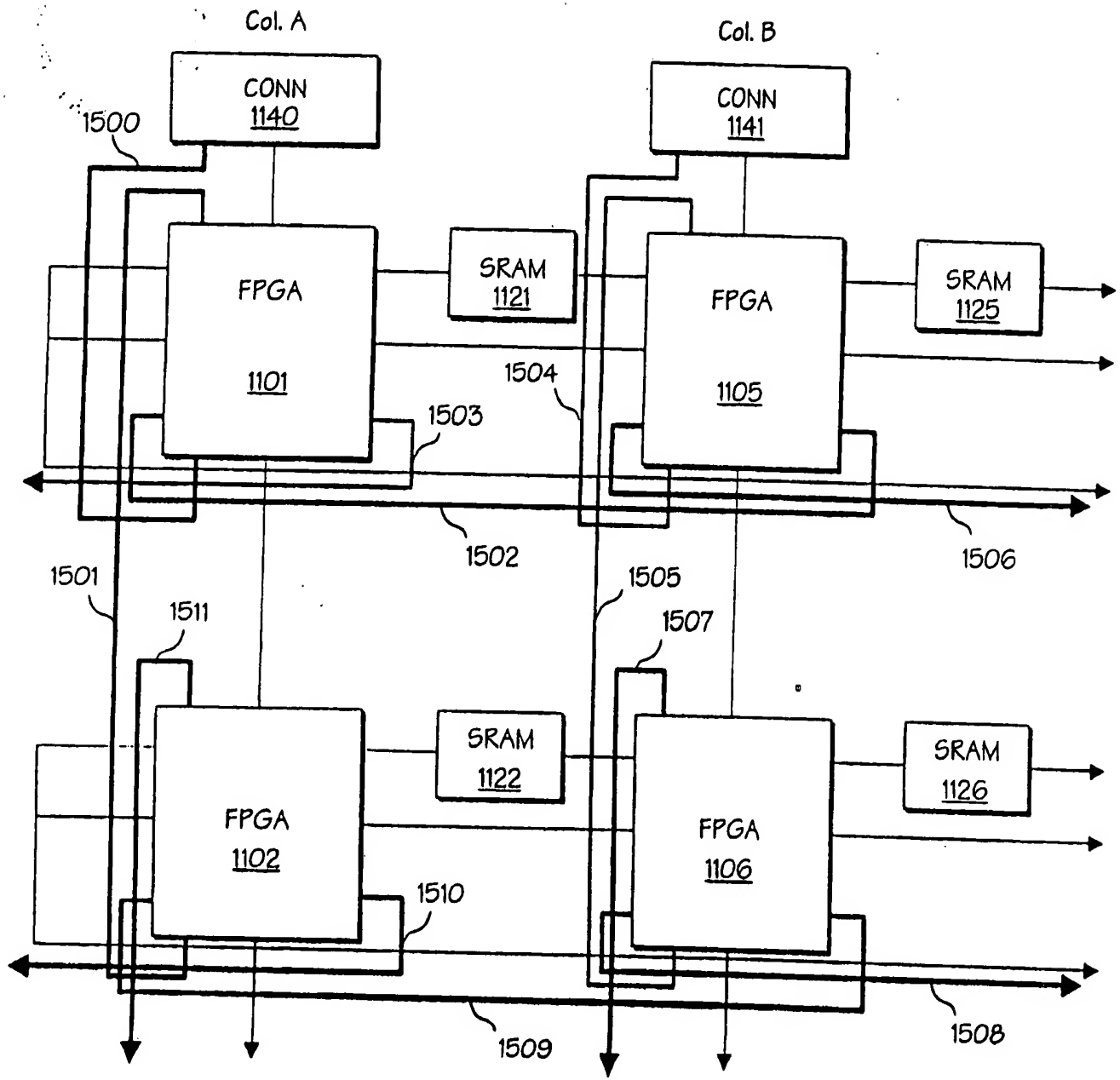

Col. A
Col. B
CONN
1140
CONN
1141
1500
FPGA
1101
SRAM
1121
FPGA
1105
SRAM
1125
1504
1503
1502
1506
1501
1511
1505
1507
FPGA
1102
SRAM
1122
FPGA
1106
SRAM
1126
1510
1509
1508

FIG. 59

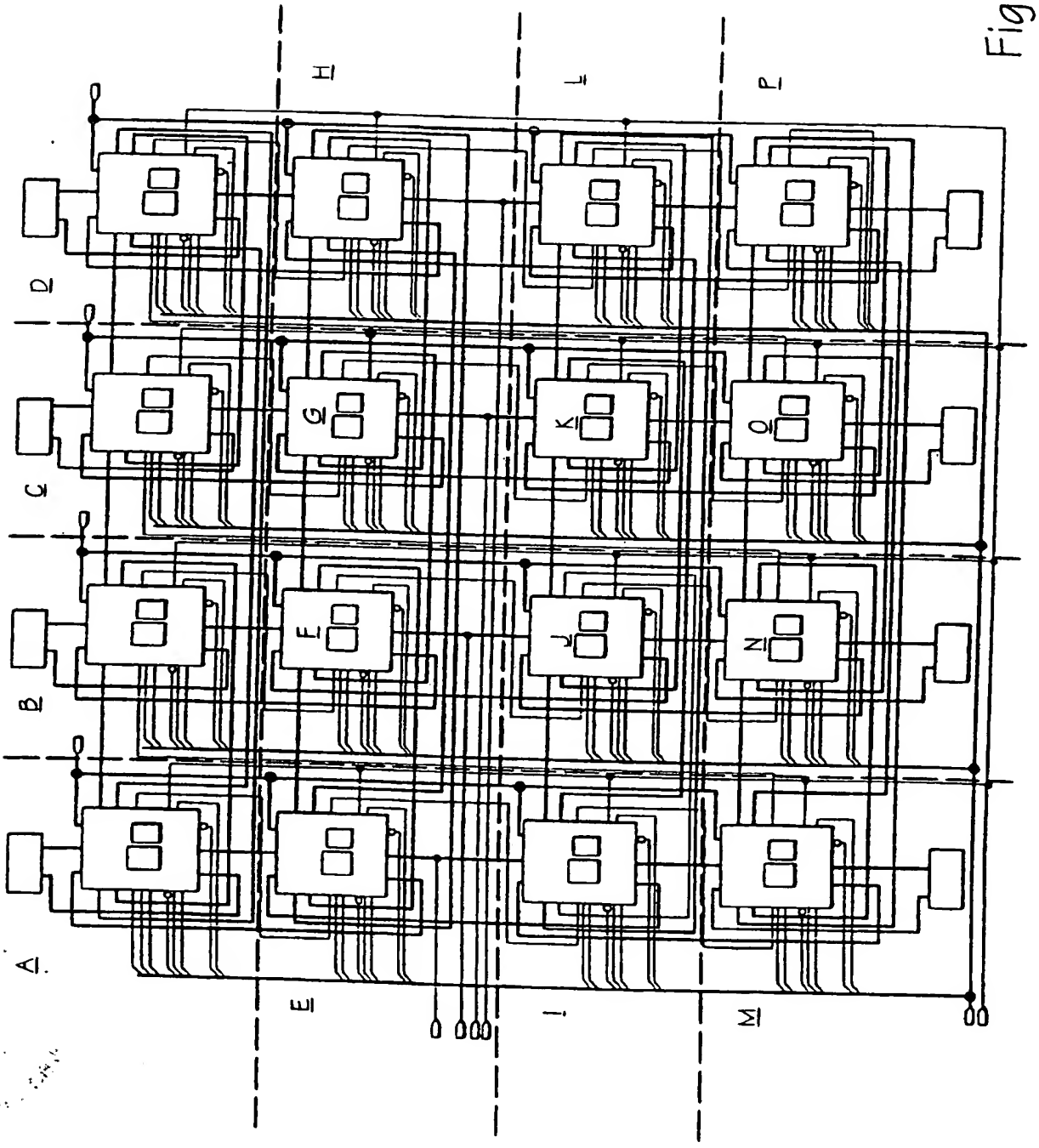
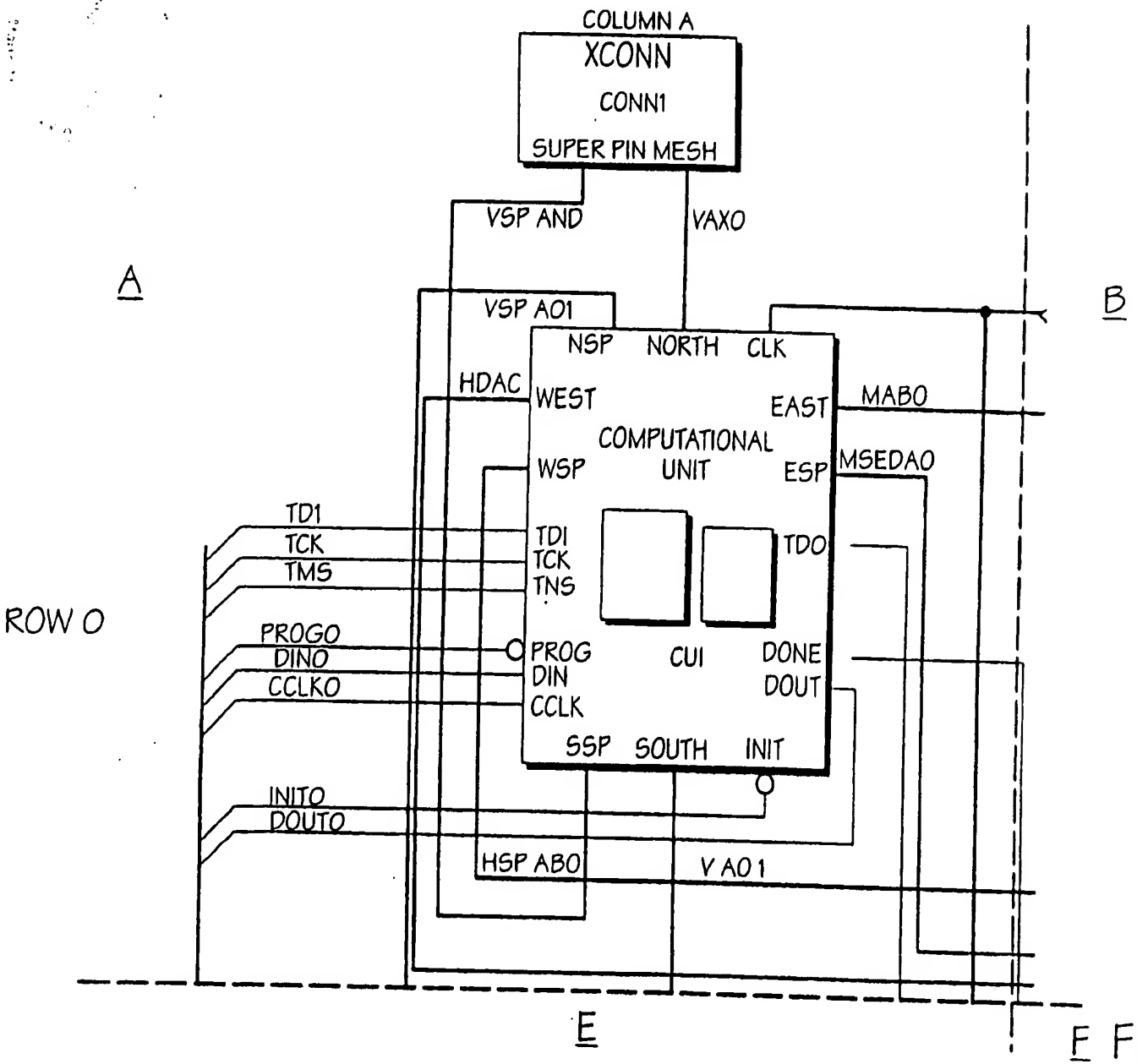


Fig. 60


COLUMN A
XCONN
CONN1
SUPER PIN MESH
VSP AND
VAXO
A
B
VSP AO1
NSP
NORTH
CLK
HDAC
WEST
EAST
MABO
COMPUTATIONAL
WSP
UNIT
ESP
MSEDAO
TD1
TCK
TMS
TDI
TCK
TNS
TDO
ROW O
PROGO
DINO
CCLKO
PROG
DIN
CCLK
CUI
DONE
DOUT
SSP
SOUTH
INIT
INITO
DOUTO
HSP ABO
V AO1
E

E Fig. 60A

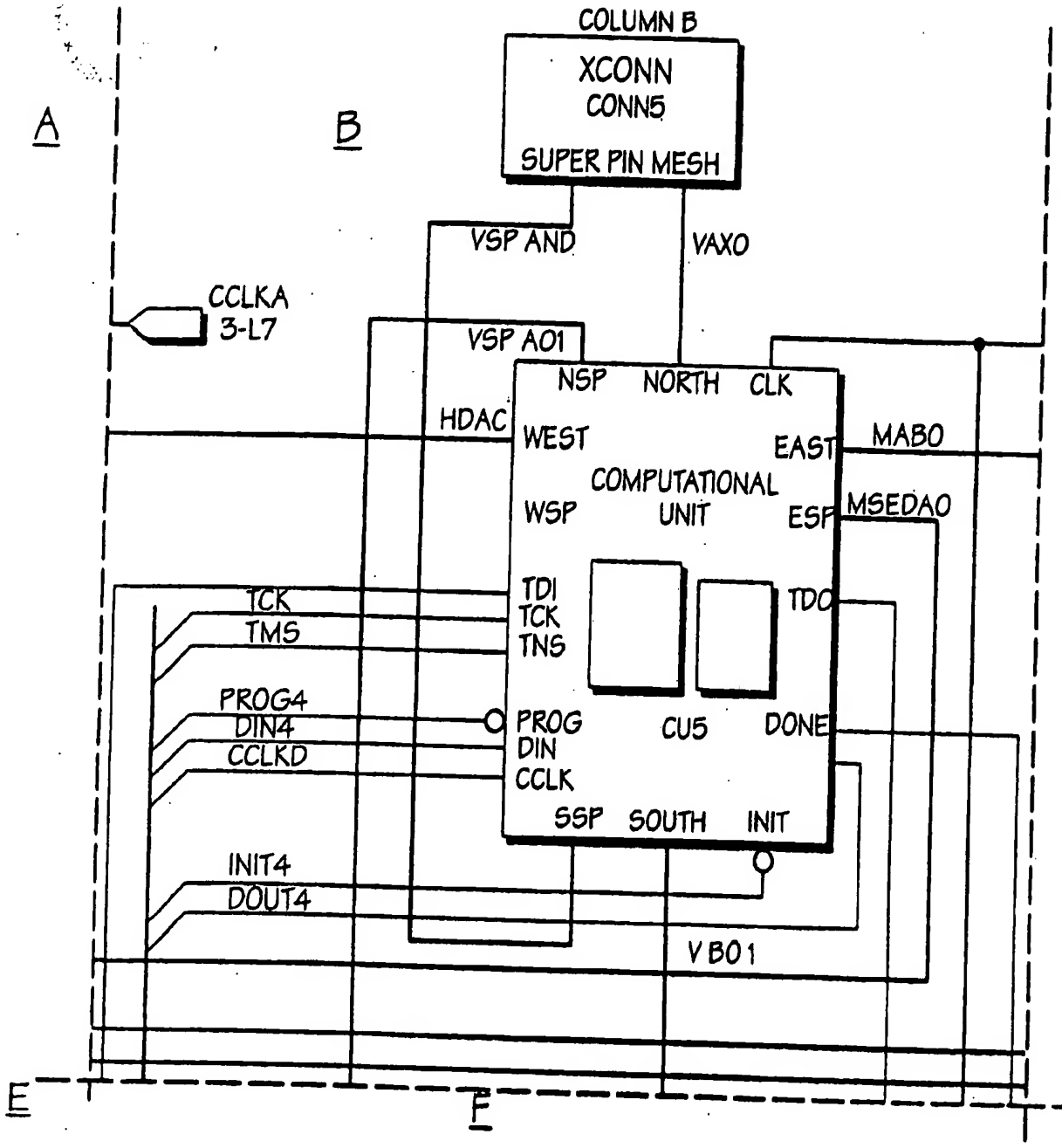

COLUMN B
XCONN
CONN5
SUPER PIN MESH
A
B
C
VSP AND
VAXO
CCLKA
3-L7
VSP A01
NSP
NORTH
CLK
HDAC
WEST
EAST
MABO
COMPUTATIONAL
WSP
UNIT
ESP
MSEDAO
TDI
TCK
TNS
TDO
TCK
TMS
PROG4
DIN4
CCLKD
PROG
DIN
CCLK
CU5
DONE
SSP
SOUTH
INIT
INIT4
DOUT4
VB01
E
F
G

Fig. 60B

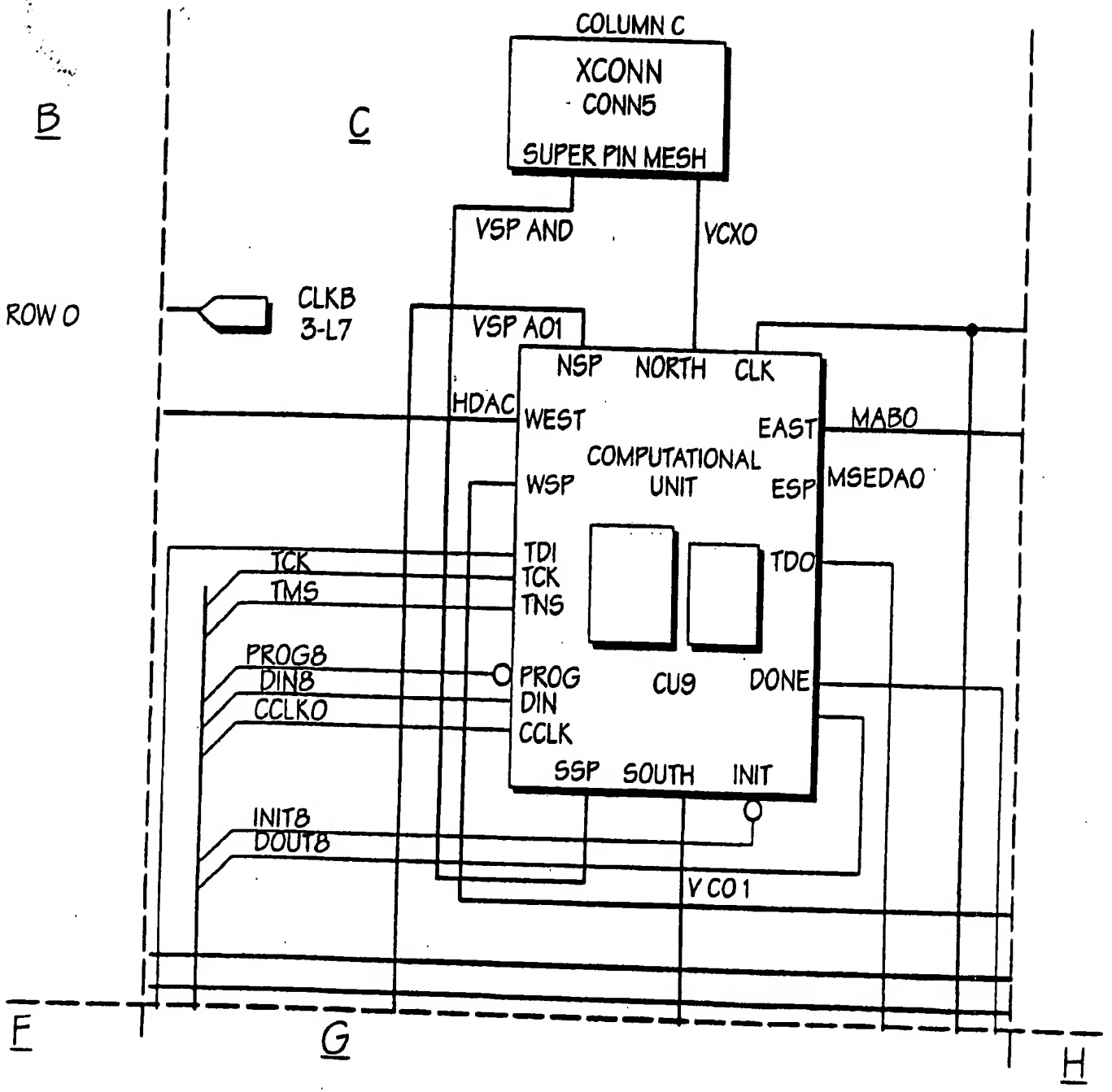

COLUMN C
XCONN
CONN5
SUPER PIN MESH
B
C
D
VSP AND
VCXO
ROW 0
CLKB
3-L7
VSP A01
NSP
NORTH
CLK
HDAC
WEST
EAST
MABO
COMPUTATIONAL
UNIT
WSP
ESP
MSEDAO
TDI
TCK
TNS
TDO
TCK
TMS
PROG8
DIN8
CCLKO
PROG
DIN
CCLK
CU9
DONE
SSP
SOUTH
INIT
INIT8
DOUT8
V CO 1
F
G
H

Fig. 60C

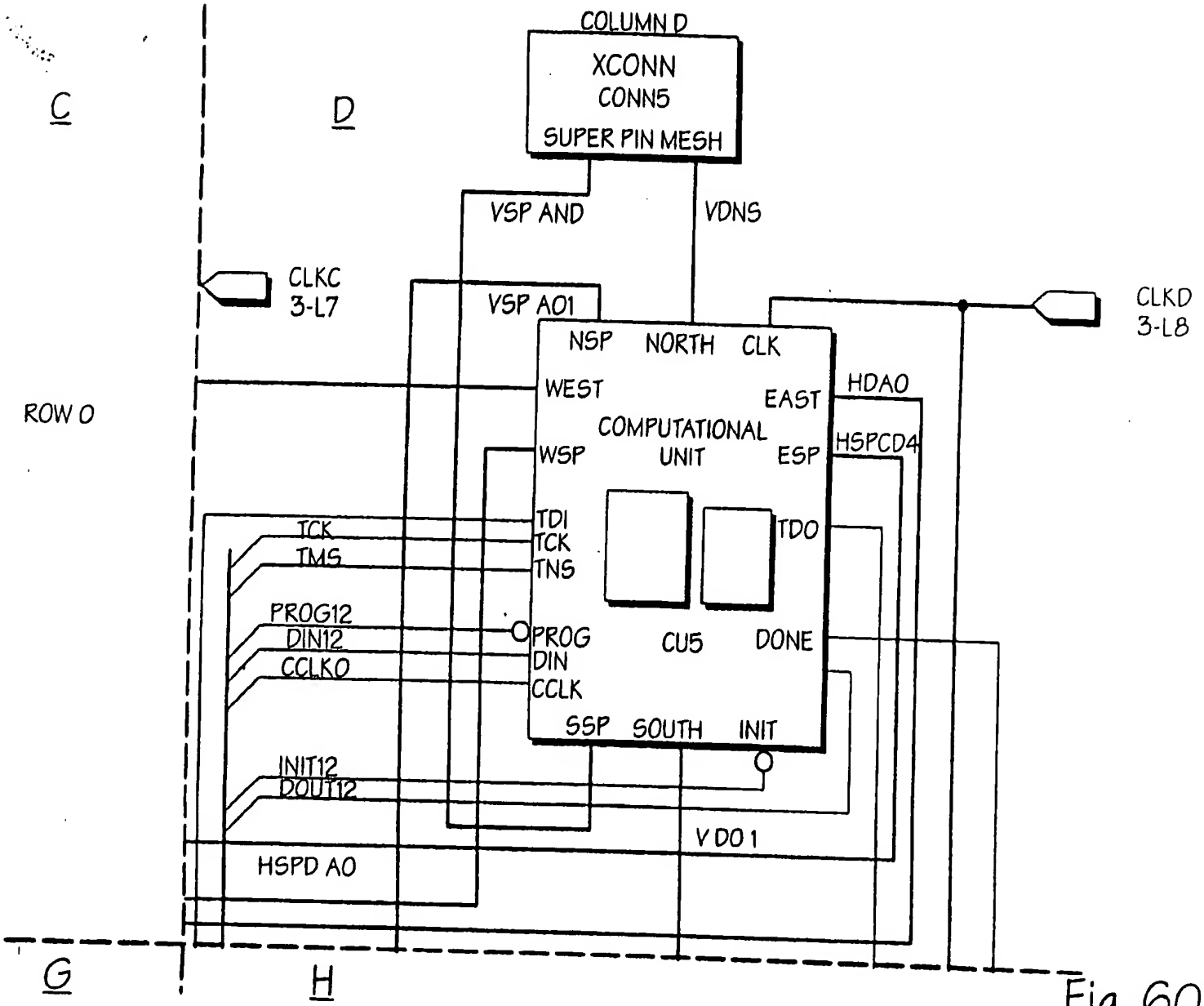

COLUMN D
XCONN
CONN5
SUPER PIN MESH
C
D
VSP AND
VDNS
CLKC
3-L7
VSP AO1
CLKD
3-L8
NSP
NORTH
CLK
WEST
EAST
HDAO
ROW O
COMPUTATIONAL
UNIT
WSP
ESP
HSPCD4
TDI
TCK
TNS
TDO
TCK
TMS
PROG12
DIN12
CCLKO
PROG
DIN
CCLK
CU5
DONE
SSP
SOUTH
INIT
INIT12
DOUT12
V DO 1
HSPD AO
G
H

Fig. 60D

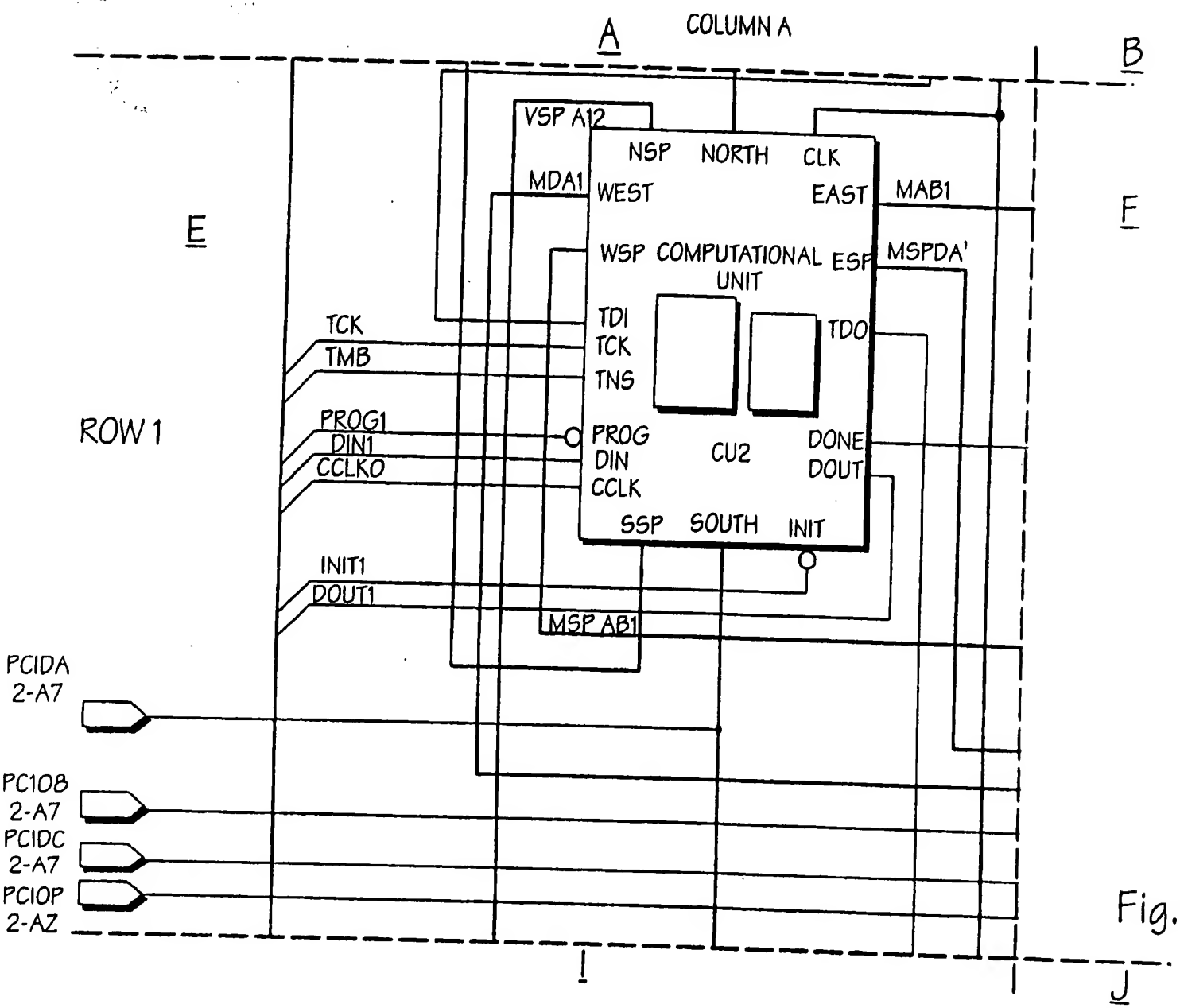

A
COLUMN A
B
E
F
ROW 1
VSP A12
NSP
NORTH
CLK
MDA1
WEST
EAST
MAB1
WSP
COMPUTATIONAL
UNIT
ESP
MSPDA'
TDI
TCK
TNS
TDO
TCK
TMB
PROG1
DIN1
CCLKO
PROG
DIN
CCLK
CU2
DONE
DOUT
SSP
SOUTH
INIT
INIT1
DOUT1
MSP AB1
PCIDA
2-A7
PC10B
2-A7
PCIDC
2-A7
PC10P
2-AZ
I
J

Fig. 60E

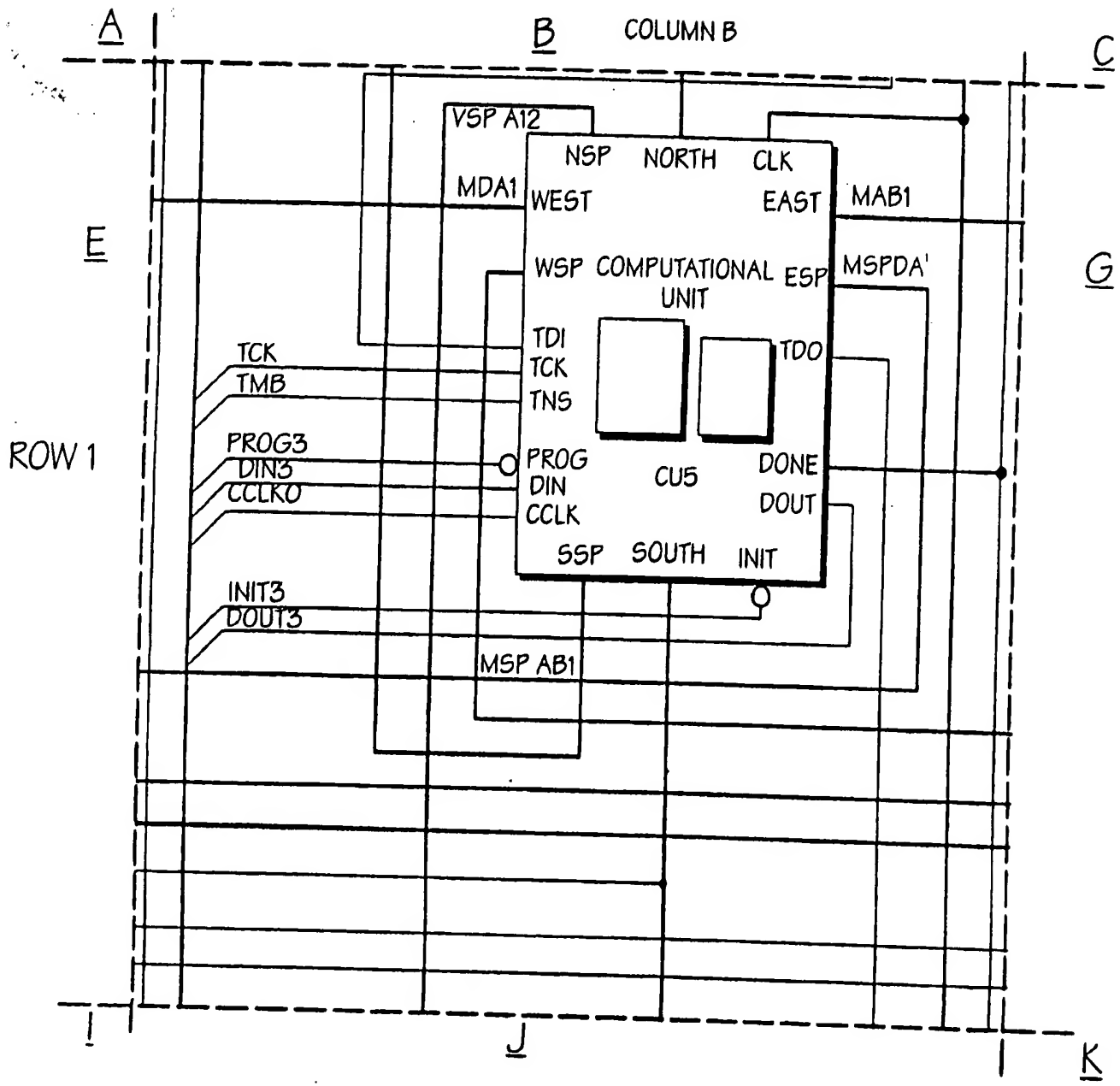

A
B
COLUMN B
C
E
G
ROW 1
I
J
K
VSP A12
NSP
NORTH
CLK
MDA1
WEST
EAST
MAB1
WSP
COMPUTATIONAL
UNIT
ESP
MSPDA'
TDI
TCK
TNS
TDO
TCK
TMB
PROG3
DIN3
CCLKO
PROG
DIN
CCLK
CU5
DONE
DOUT
SSP
SOUTH
INIT
INIT3
DOUT3
MSP AB1

Fig. 60F

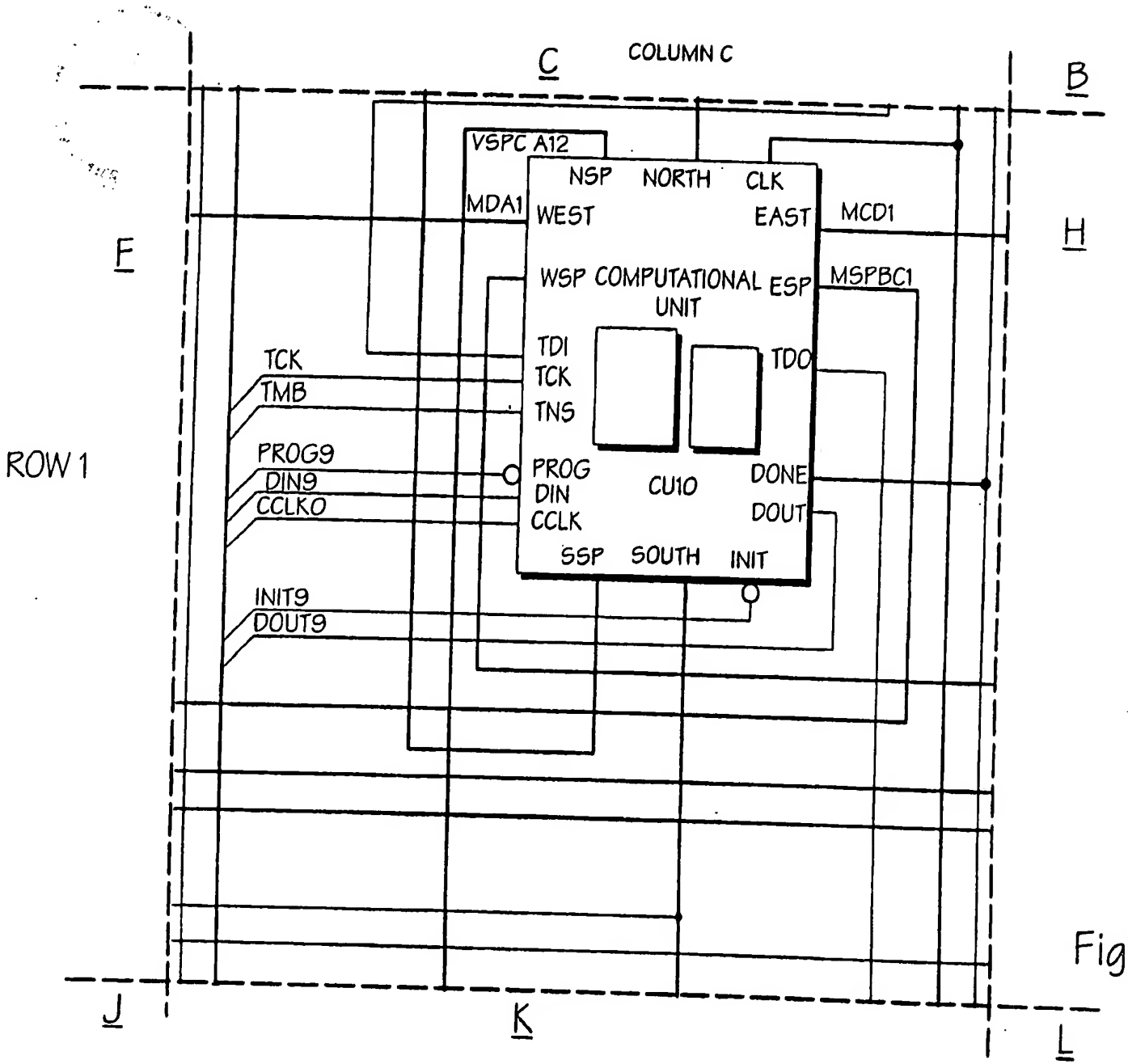

C
COLUMN C
B
VSPC A12
NSP
NORTH
CLK
MDA1
WEST
EAST
MCD1
F
H
WSP
COMPUTATIONAL
UNIT
ESP
MSPBC1
TDI
TCK
TMS
TDO
TCK
TMB
PROG9
DIN9
CCLKO
ROW 1
PROG
DIN
CCLK
CU10
DONE
DOUT
SSP
SOUTH
INIT
INIT9
DOUT9
J
K
L

Fig. 60G

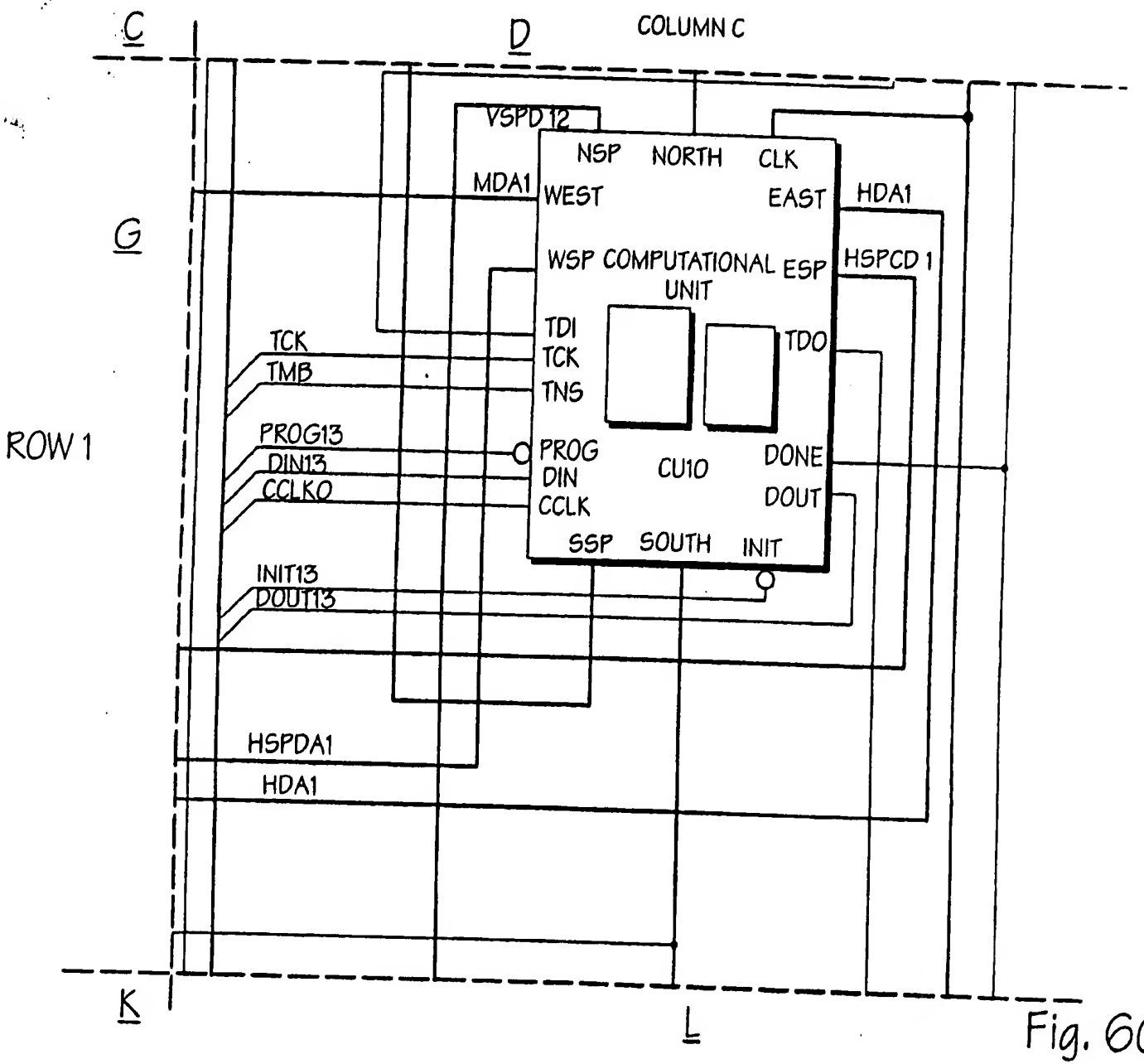

C
D
COLUMN C
G
ROW 1
K
L
VSPD12
NSP
NORTH
CLK
MDA1
WEST
EAST
HDA1
WSP
COMPUTATIONAL
UNIT
ESP
HSPCD 1
TDI
TCK
TMS
TDO
TCK
TMB
PROG13
DIN13
CCLKO
PROG
DIN
CCLK
CU10
DONE
DOUT
SSP
SOUTH
INIT
INIT13
DOUT13
HSPDA1
HDA1

Fig. 60H

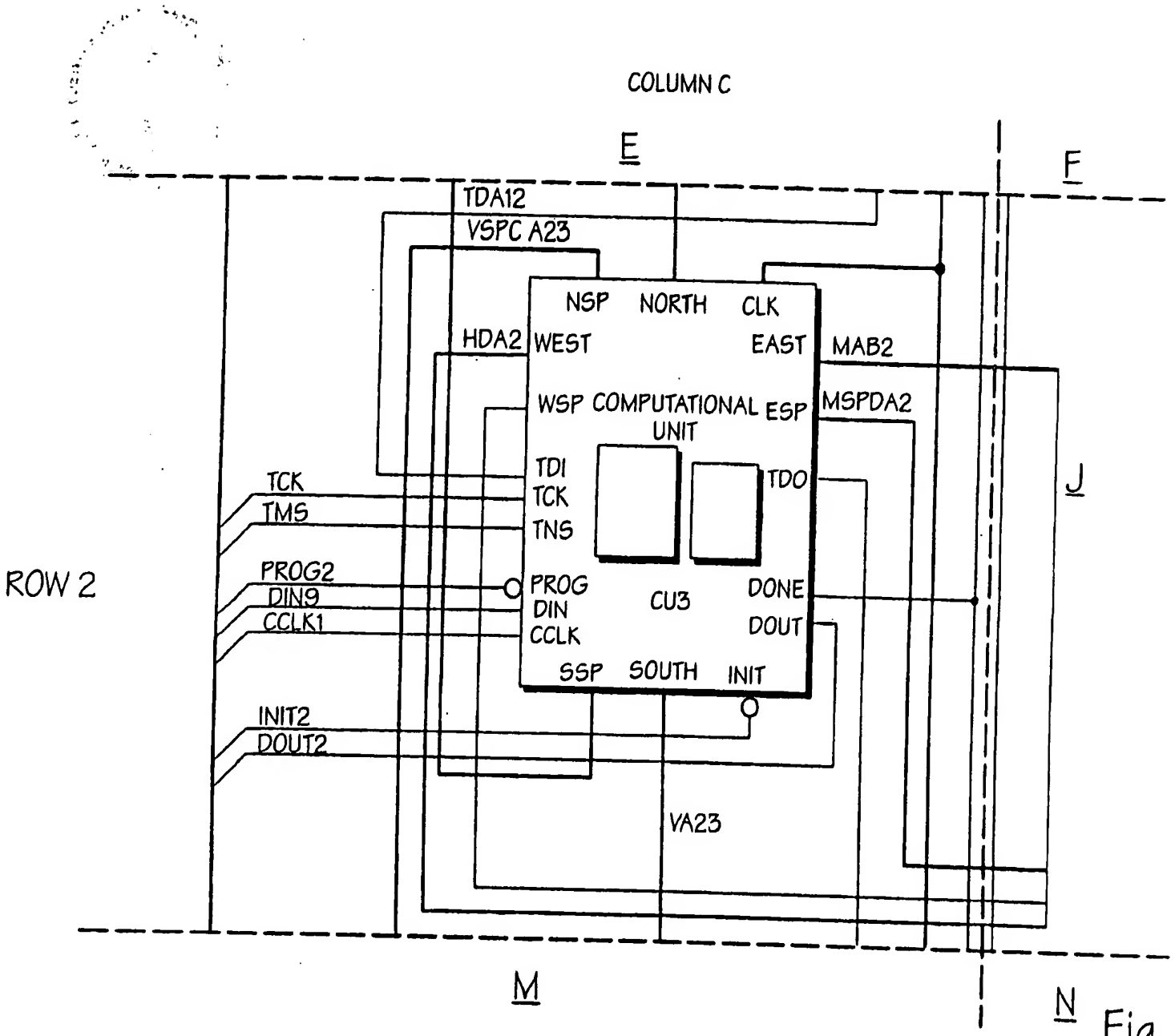

COLUMN C
E
F
TDA12
VSPC A23
NSP
NORTH
CLK
HDA2
WEST
EAST
MAB2
WSP
COMPUTATIONAL
UNIT
ESP
MSPDA2
TDI
TCK
TNS
TDO
J
TCK
TMS
ROW 2
PROG2
DIN9
CCLK1
PROG
DIN
CCLK
CU3
DONE
DOUT
SSP
SOUTH
INIT
INIT2
DOUT2
VA23
M
N

Fig. 601

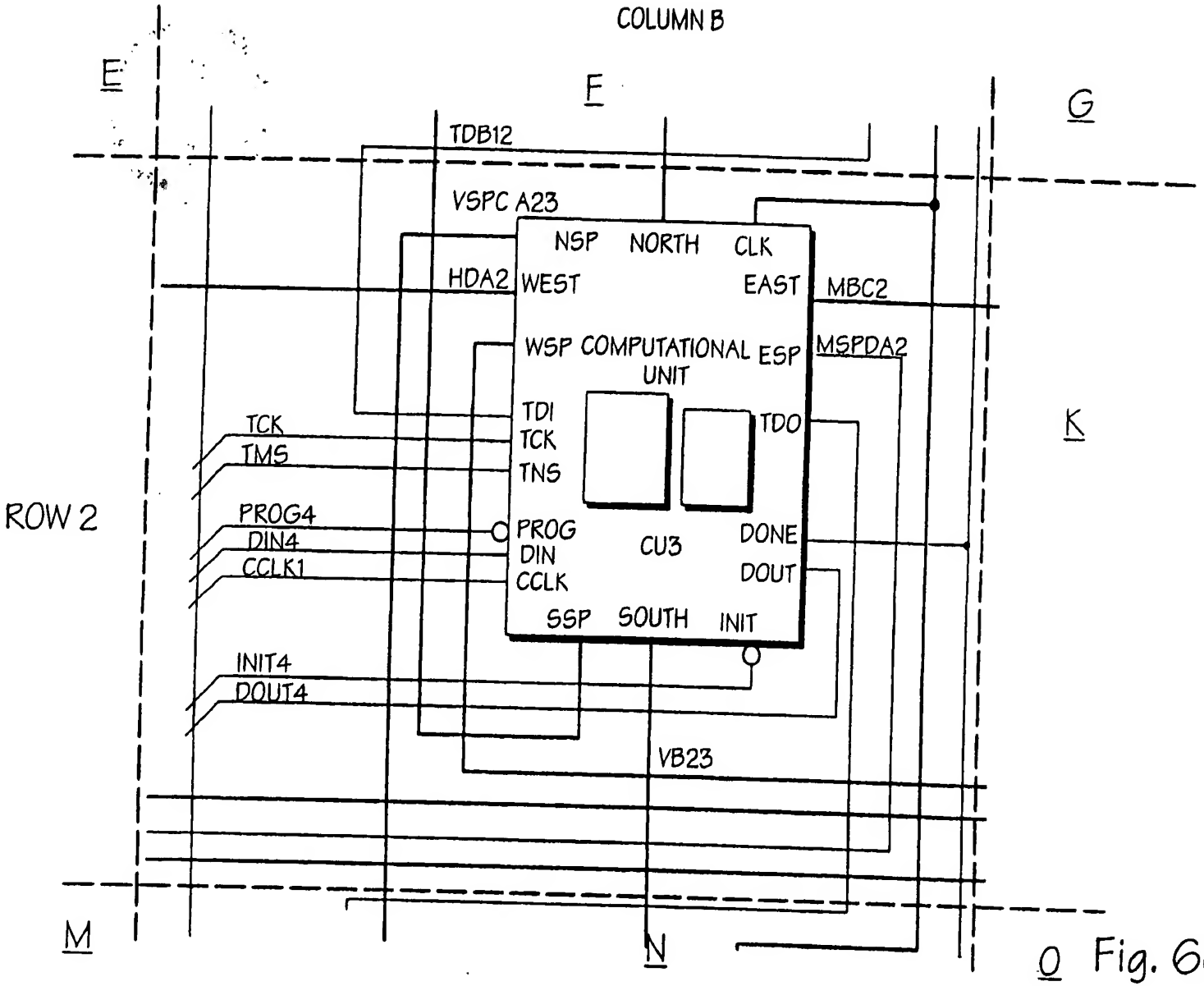

COLUMN B
E
F
G
TDB12
VSPC A23
NSP
NORTH
CLK
HDA2
WEST
EAST
MBC2
WSP
COMPUTATIONAL
UNIT
ESP
MSPDA2
TDI
TCK
TNS
TDO
K
TCK
TMS
ROW 2
PROG4
DIN4
CCLK1
PROG
DIN
CCLK
CU3
DONE
DOUT
SSP
SOUTH
INIT
INIT4
DOUT4
VB23
M
N
O

Fig. 60J

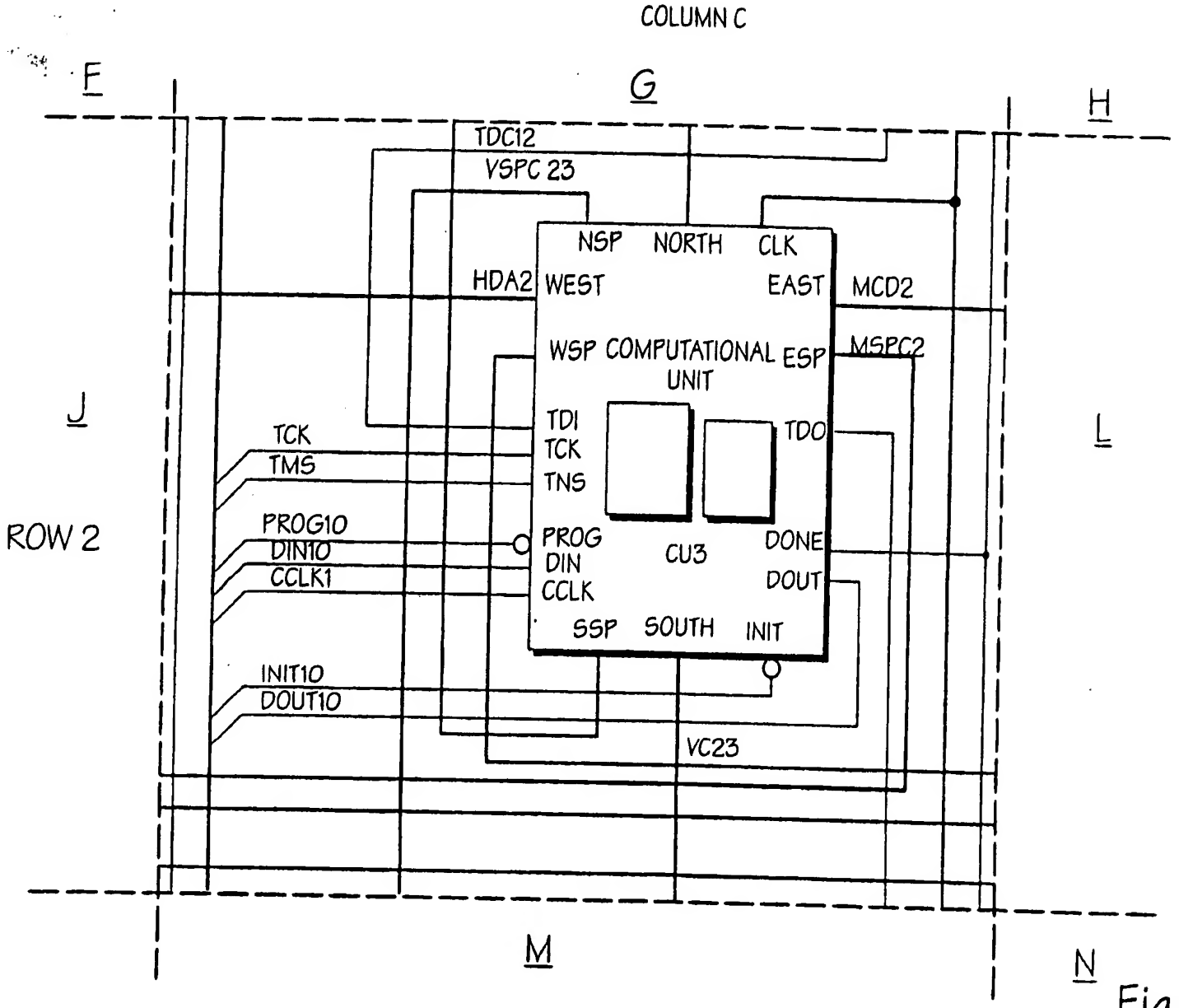

COLUMN C
F
G
H
J
L
M
N
ROW 2
TDC12
VSPC 23
NSP
NORTH
CLK
HDA2
WEST
EAST
MCD2
WSP
COMPUTATIONAL UNIT
ESP
MSPC2
TDI
TCK
TNS
TDO
TCK
TMS
PROG10
DIN10
CCLK1
PROG
DIN
CCLK
CU3
DONE
DOUT
SSP
SOUTH
INIT
INIT10
DOUT10
VC23

Fig. 60K

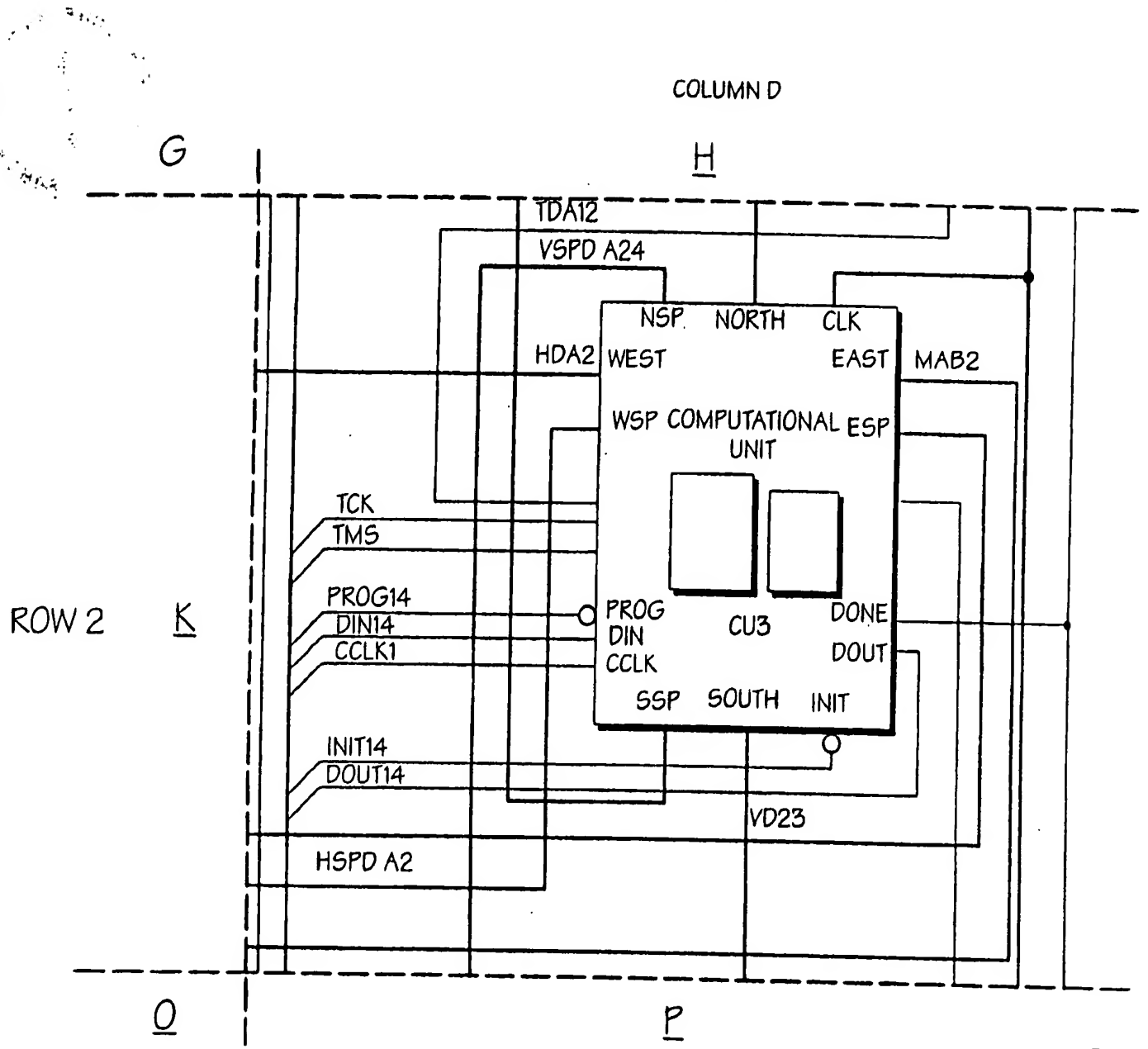

COLUMN D
G
H
TDA12
VSPD A24
NSP
NORTH
CLK
HDA2
WEST
EAST
MAB2
WSP
COMPUTATIONAL UNIT
ESP
TCK
TMS
PROG14
DIN14
CCLK1
ROW 2
K
PROG
DIN
CCLK
CU3
DONE
DOUT
SSP
SOUTH
INIT
INIT14
DOUT14
VD23
HSPD A2
O
P

Fig. 60L

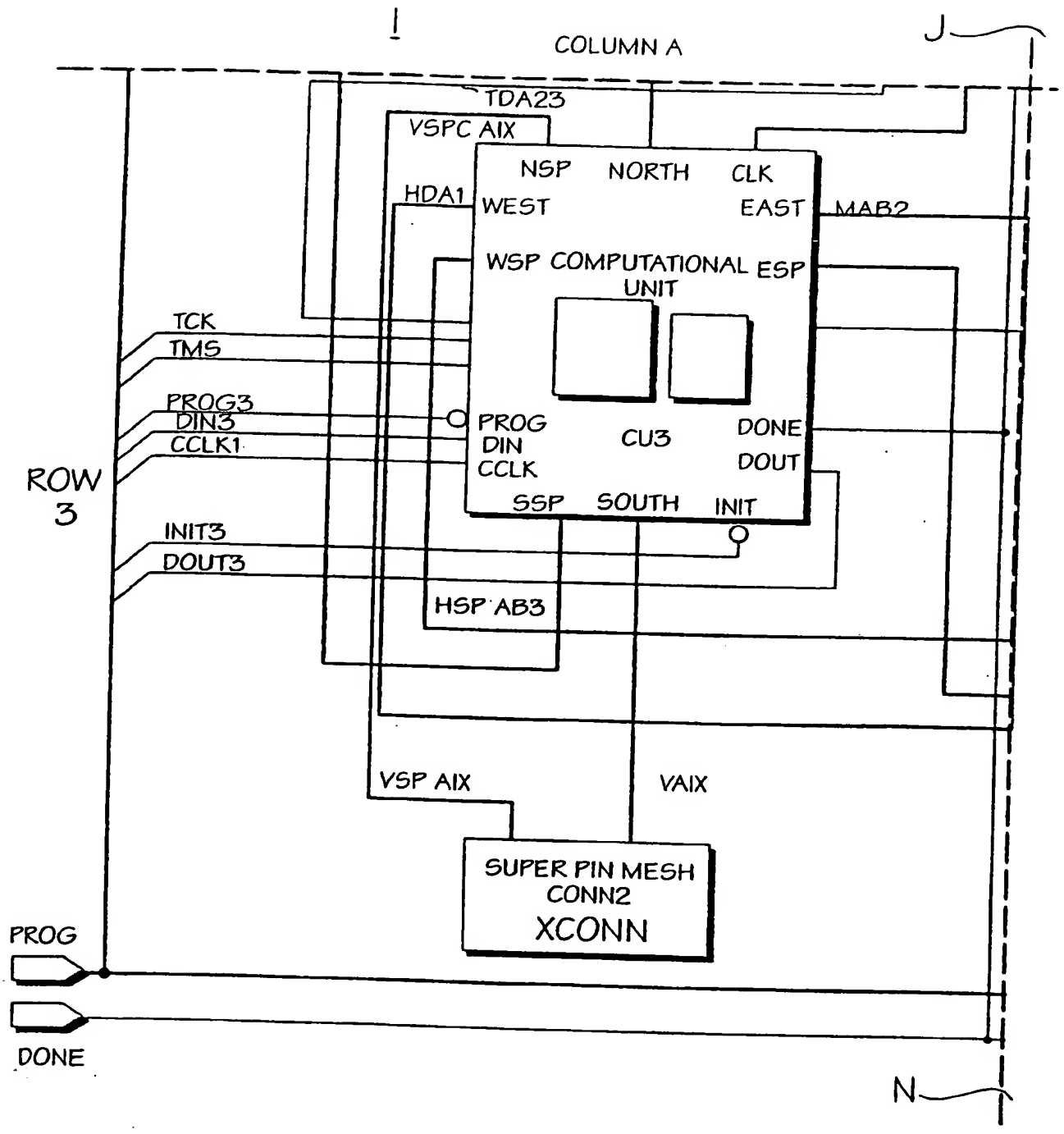

I
COLUMN A
J
TDA23
VSPC AIX
NSP
NORTH
CLK
HDA1
WEST
EAST
MAB2
WSP
COMPUTATIONAL
UNIT
ESP
TCK
TMS
PROG3
DIN3
CCLK1
ROW
3
PROG
DIN
CCLK
CU3
DONE
DOUT
SSP
SOUTH
INIT
INIT3
DOUT3
HSP AB3
VSP AIX
VAIX
SUPER PIN MESH
CONN2
XCONN
PROG
DONE
N

Fig. 60M

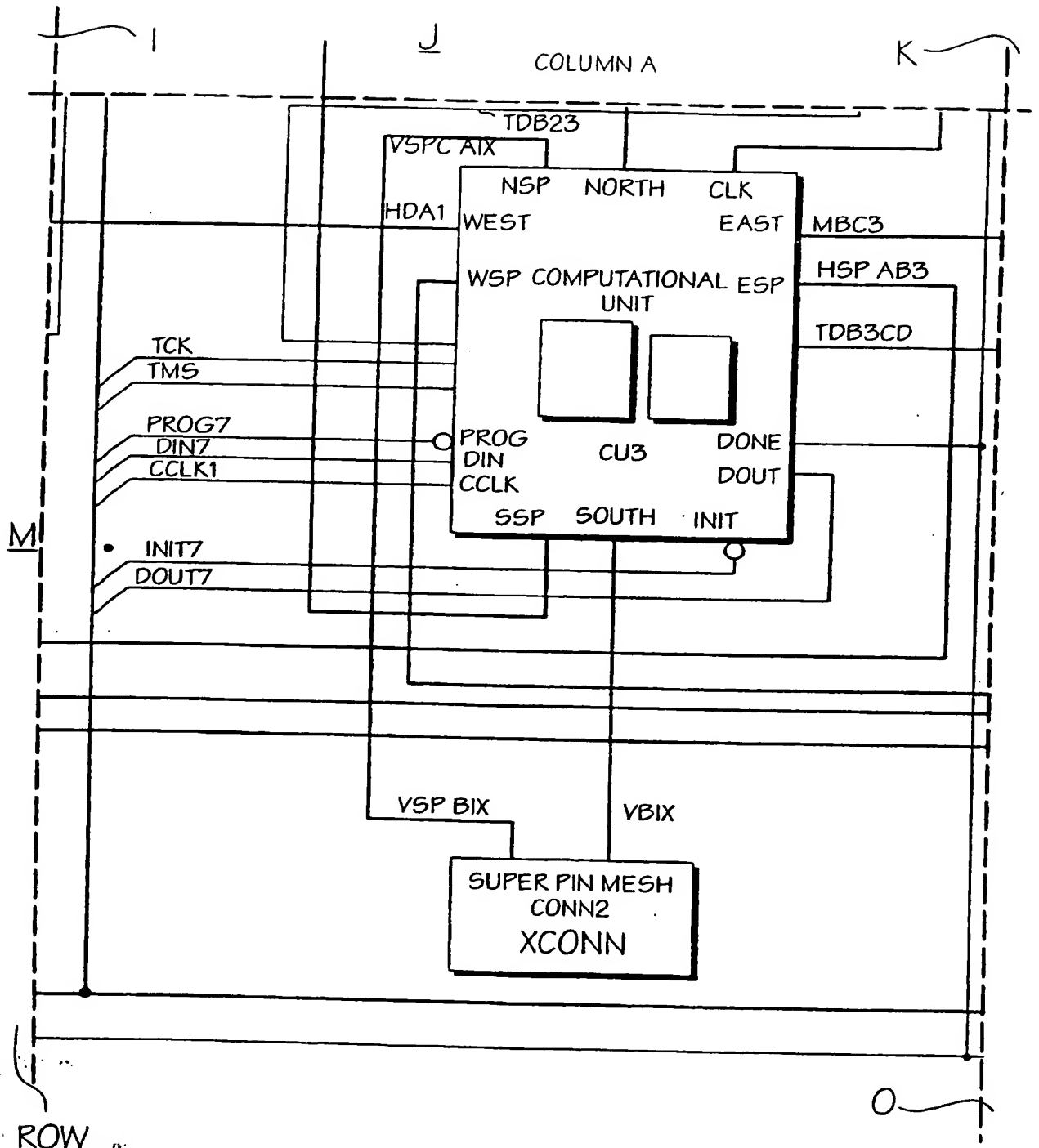

I
J
K
COLUMN A
TDB23
VSPC AIX
NSP
NORTH
CLK
HDA1
WEST
EAST
MBC3
WSP
COMPUTATIONAL UNIT
ESP
HSP AB3
TDB3CD
TCK
TMS
PROG7
DIN7
CCLK1
PROG
DIN
CCLK
CU3
DONE
DOUT
SSP
SOUTH
INIT
M
INIT7
DOUT7
VSP BIX
VBIX
SUPER PIN MESH
CONN2
XCONN
O
ROW
3

Fig. 60N

20120209-2980-2007

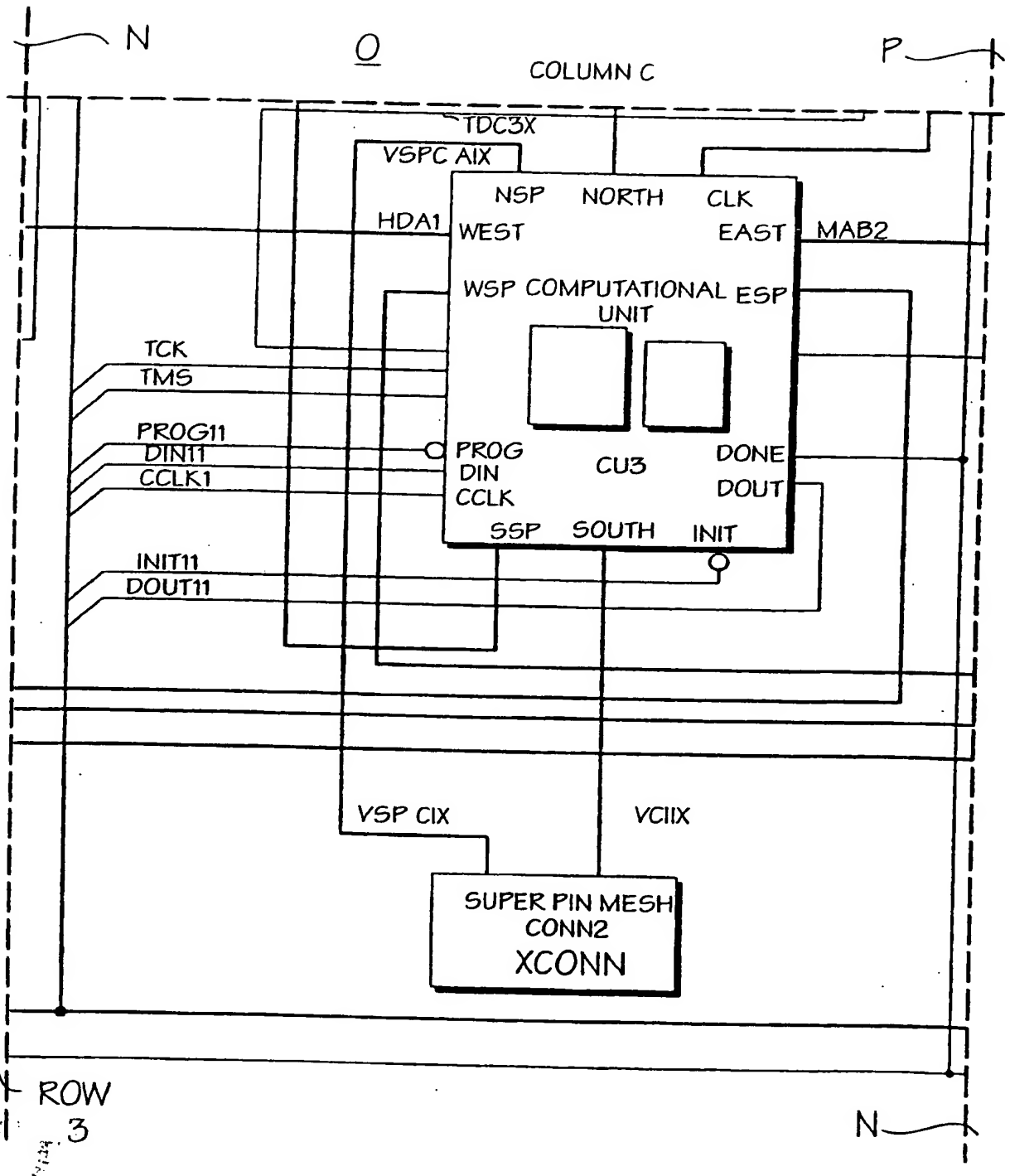


Fig. 600

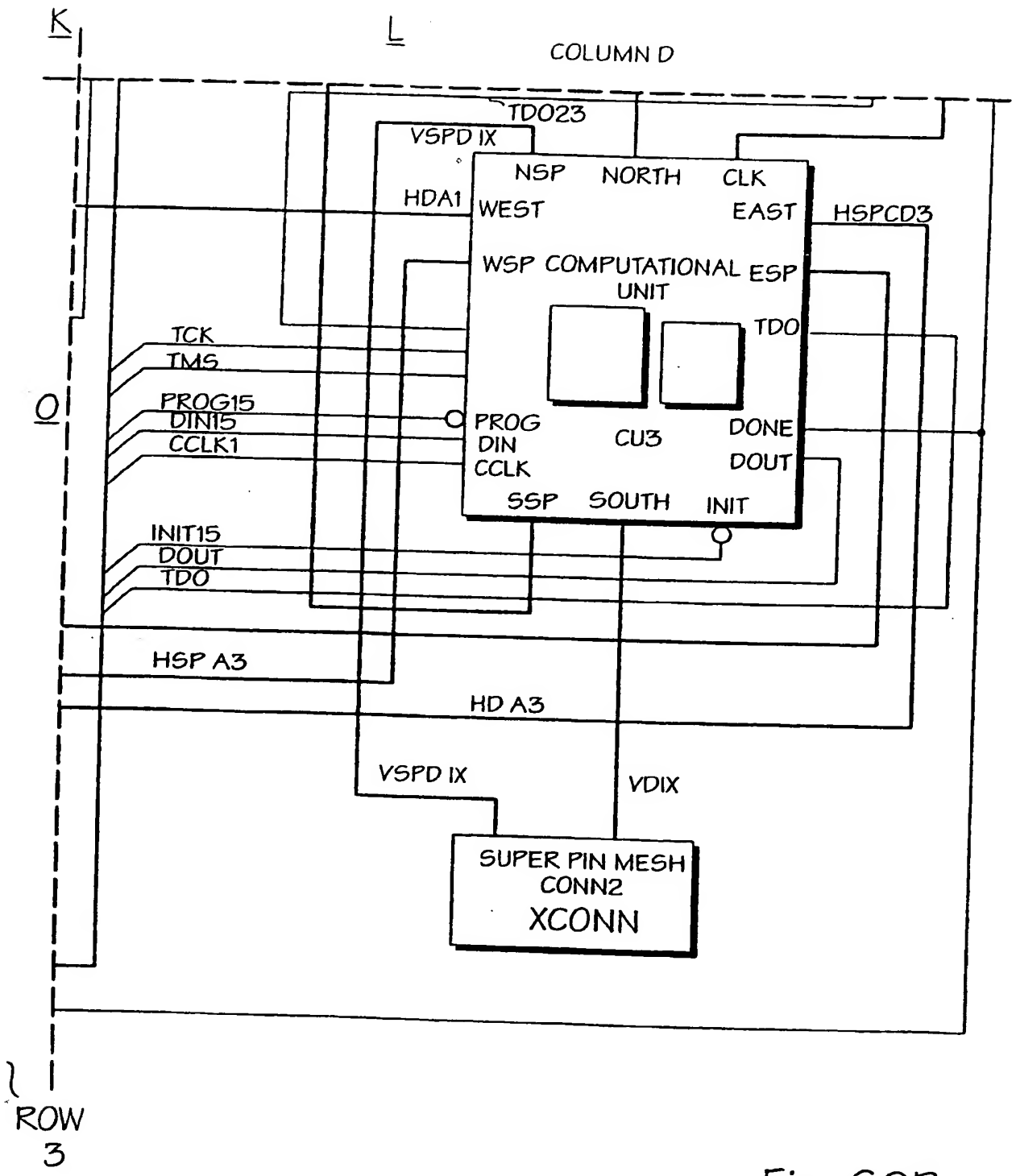

K
L
COLUMN D
TDO23
VSPD IX
NSP
NORTH
CLK
HDA1
WEST
EAST
HSPCD3
WSP
COMPUTATIONAL UNIT
ESP
TDO
TCK
TMS
O
PROG15
DIN15
CCLK1
PROG
DIN
CCLK
CU3
DONE
DOUT
SSP
SOUTH
INIT
INIT15
DOUT
TDO
HSP A3
HD A3
VSPD IX
VDIX
SUPER PIN MESH
CONN2
XCONN
ROW
3

Fig. 60P

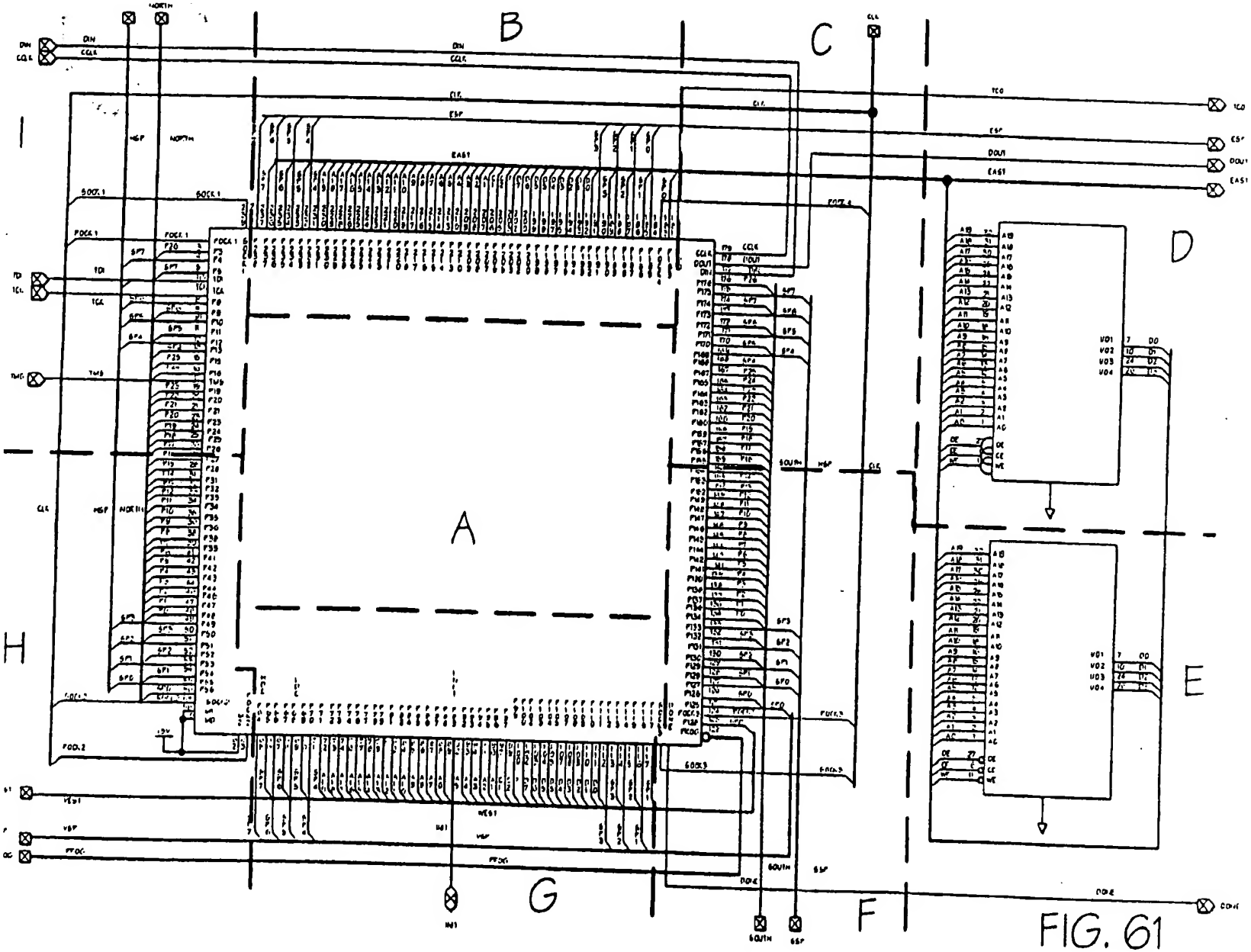


FIG. 61

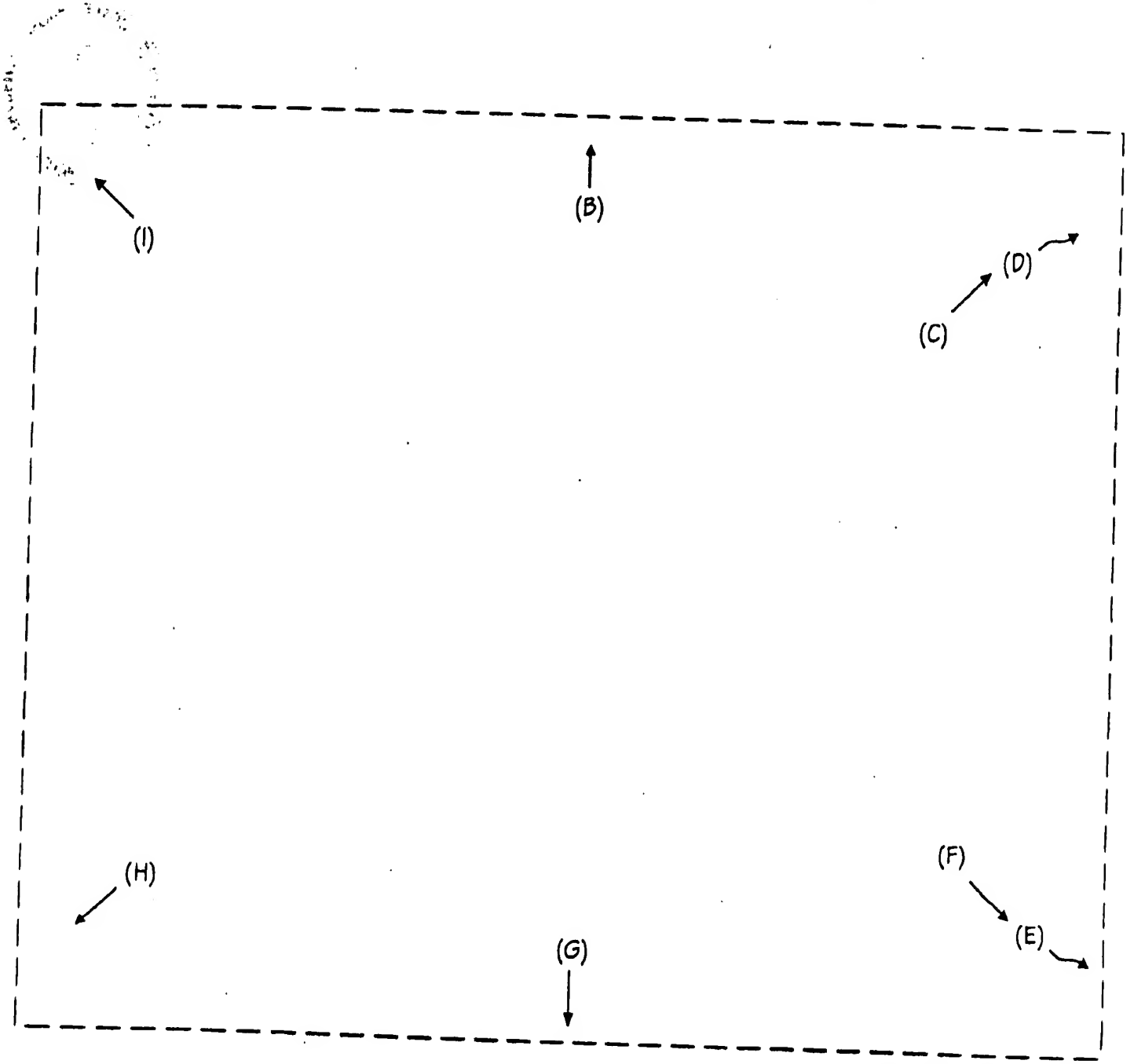


FIG. 61(A)

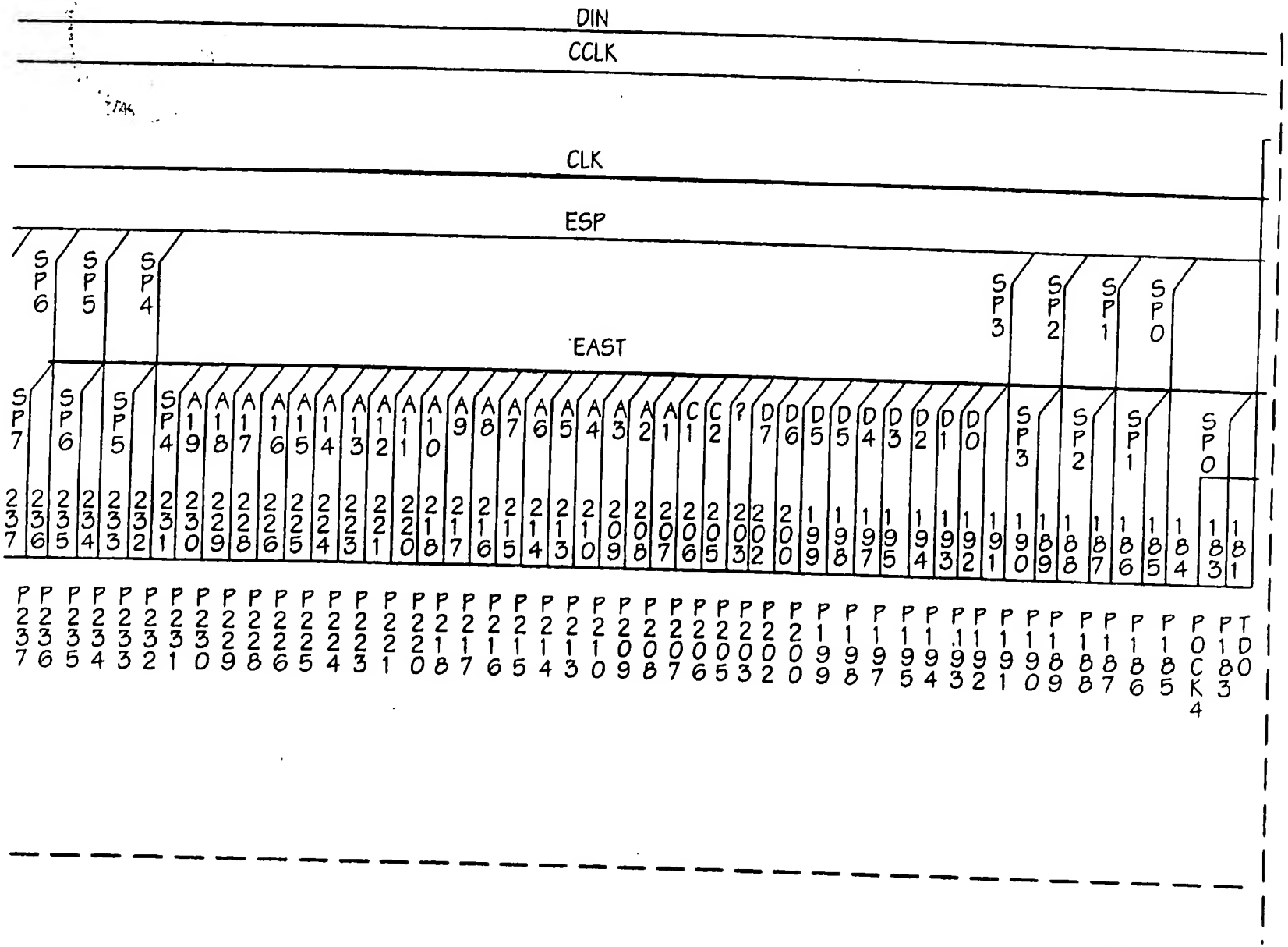
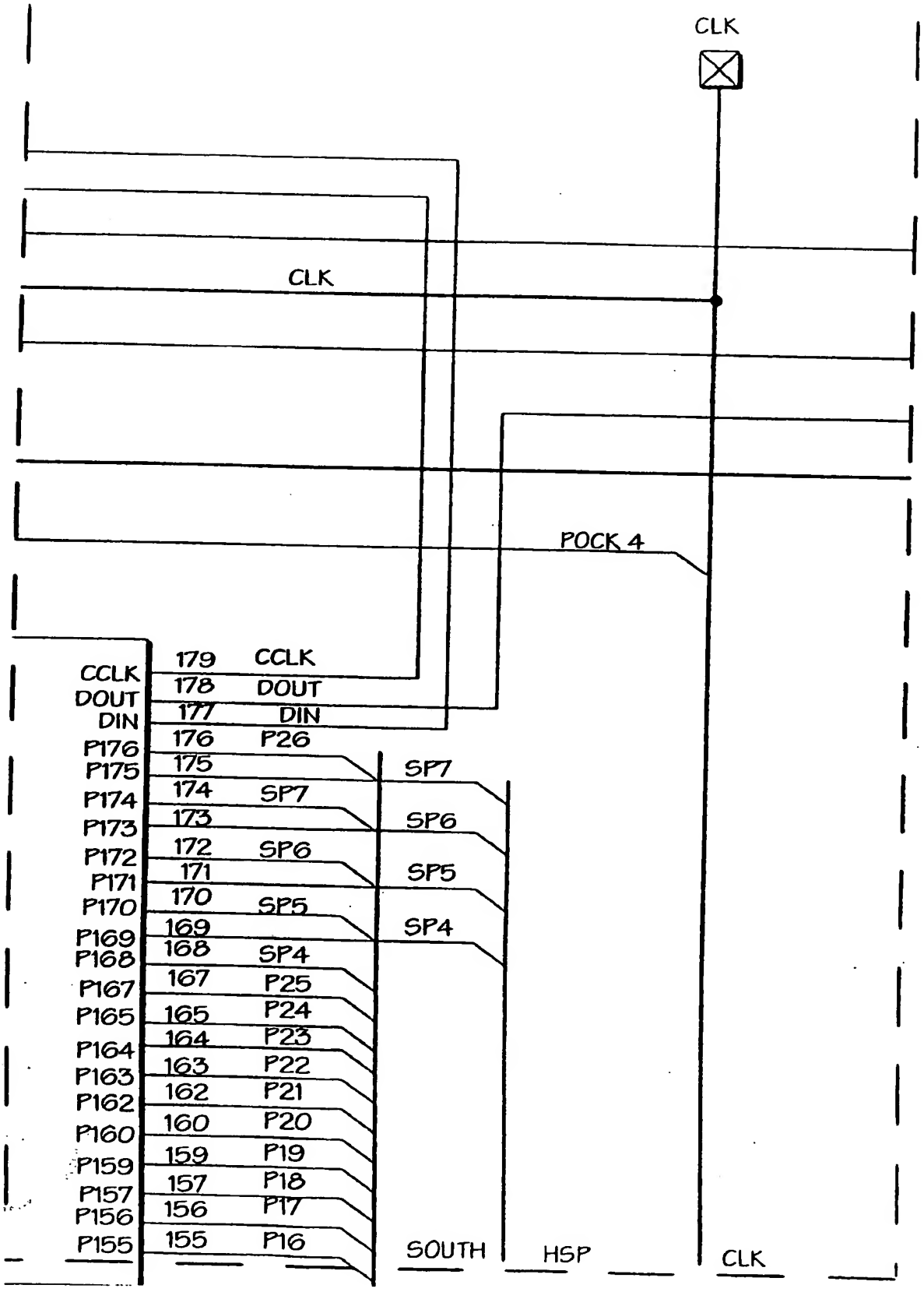

DIN
CCLK
CLK
ESP
EAST
SP6
SP5
SP4
SP3
SP2
SP1
SP0
SP7 237
SP6 236
SP5 235
SP4 234
SP5 233
SP4 232
SP4 231
A19 230
A18 229
A17 228
A16 226
A15 225
A14 224
A13 223
A12 221
A11 220
A10 218
A9 217
A8 216
A7 215
A6 214
A5 213
A4 210
A3 209
A2 208
A1 207
C1 206
C2 205
? 203
D7 202
D6 200
D5 199
D5 198
D4 197
D3 195
D2 194
D1 193
D0 192
191
SP3 190
SP2 189
SP2 188
SP1 187
SP1 186
SP0 185
184
SP0 183
181
P237
P236
P235
P234
P233
P232
P231
P230
P229
P228
P226
P225
P224
P223
P221
P220
P218
P217
P216
P215
P214
P213
P210
P209
P208
P207
P206
P205
P203
P202
P200
P199
P198
P197
P195
P194
P193
P192
P191
P190
P189
P188
P187
P186
P185
POCK4
P183
TDO

FIG. 61(B)

20120 29802001



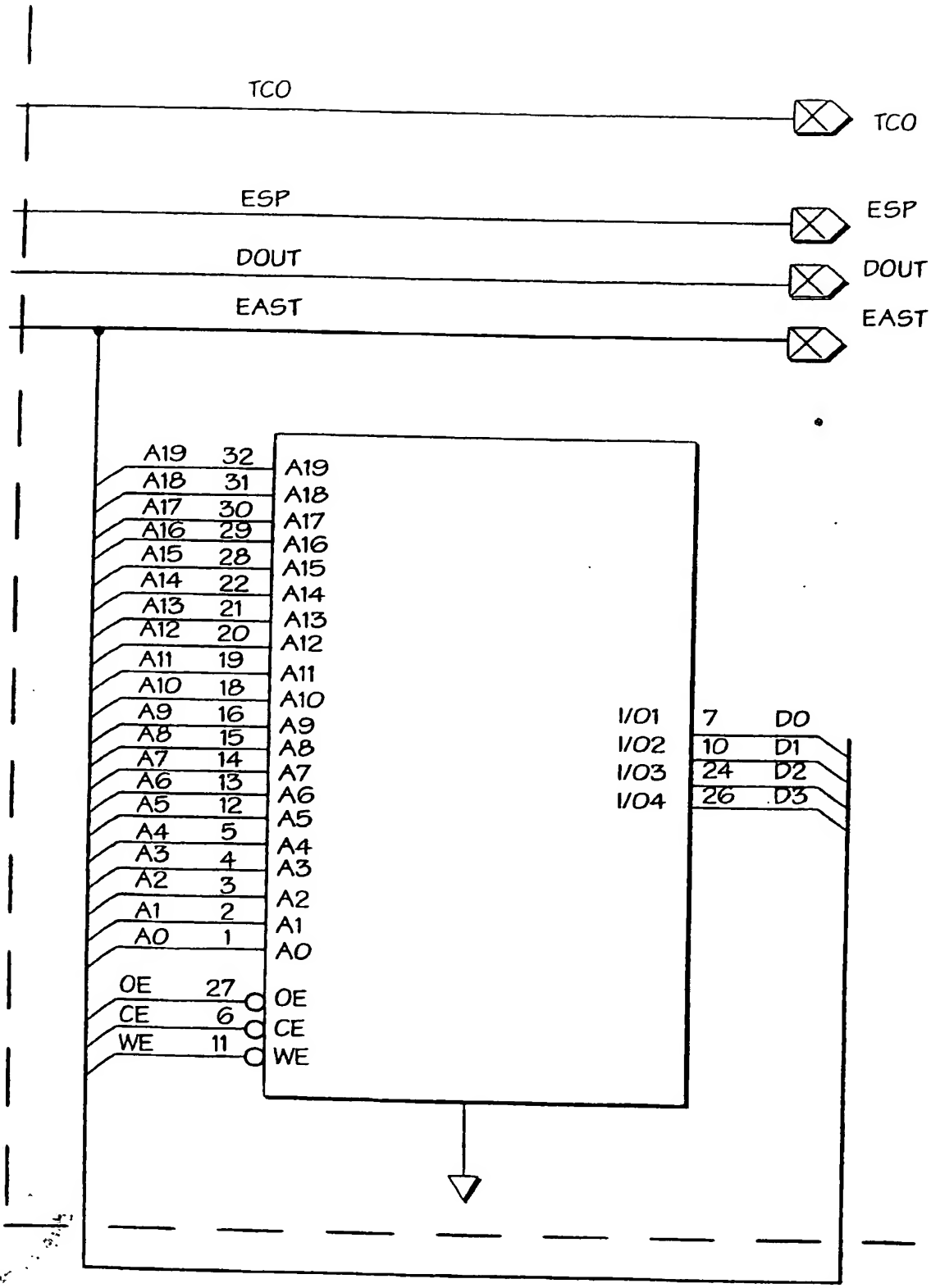

TCO
TCO
ESP
ESP
DOUT
DOUT
EAST
EAST
A19 32 A19
A18 31 A18
A17 30 A17
A16 29 A16
A15 28 A15
A14 22 A14
A13 21 A13
A12 20 A12
A11 19 A11
A10 18 A10
A9 16 A9
A8 15 A8
A7 14 A7
A6 13 A6
A5 12 A5
A4 5 A4
A3 4 A3
A2 3 A2
A1 2 A1
A0 1 A0
OE 27 OE
CE 6 CE
WE 11 WE
I/O1 7 D0
I/O2 10 D1
I/O3 24 D2
I/O4 26 D3

FIG. 61(D)

20120220-2390220T

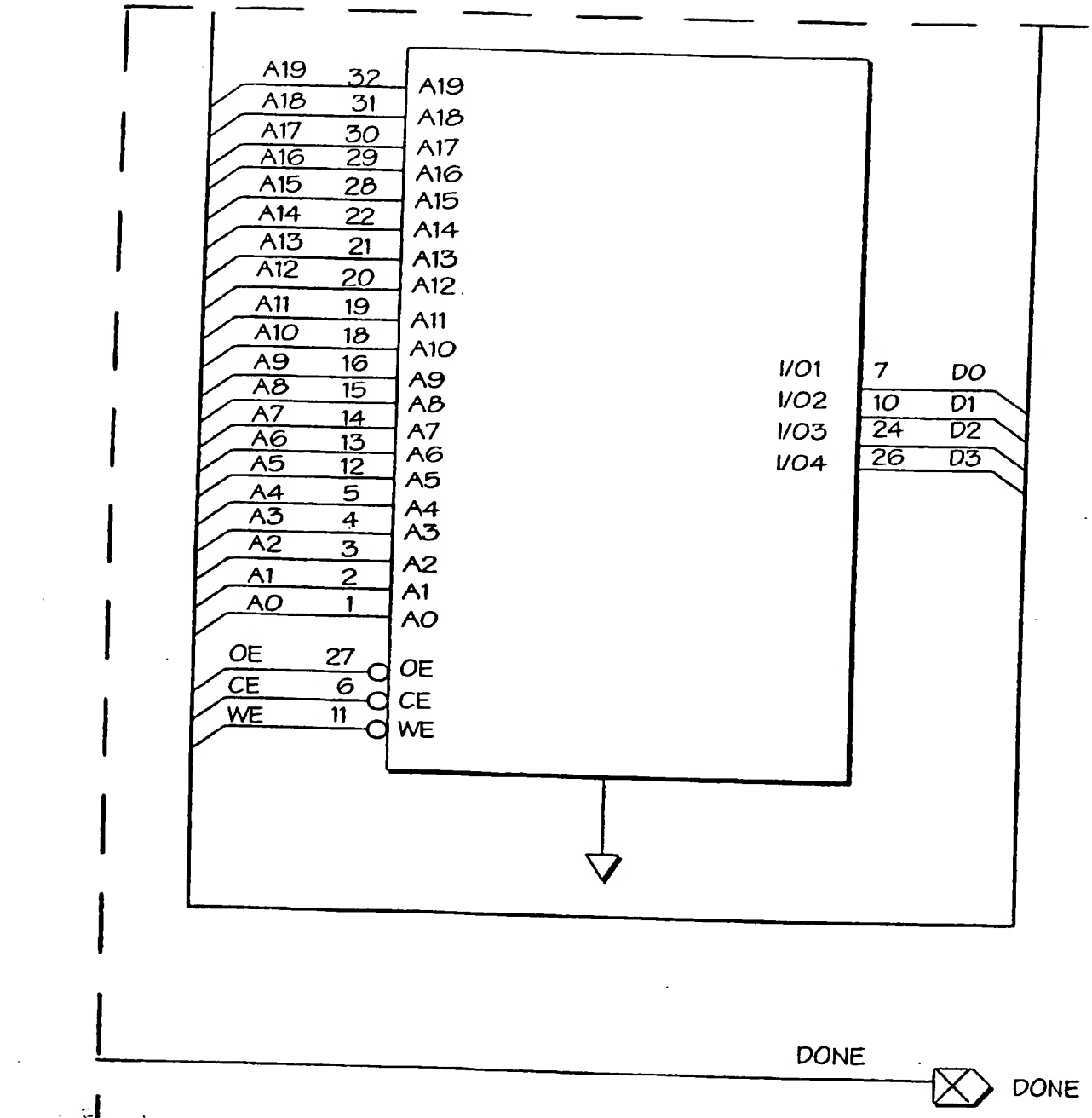


FIG. 61(E)

4,706,205 Nov. 10, 1987

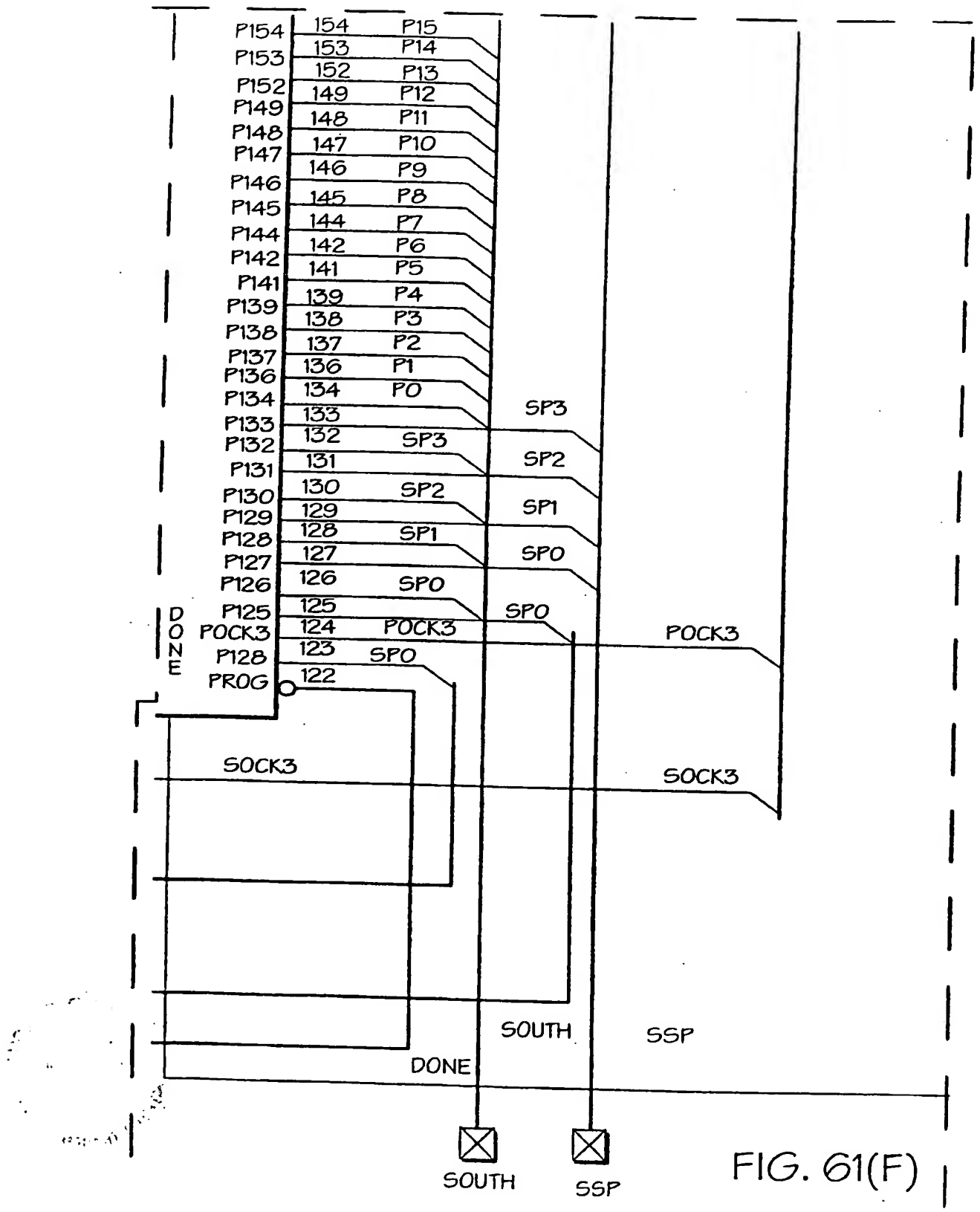


FIG. 61(F)

20T280 29802001

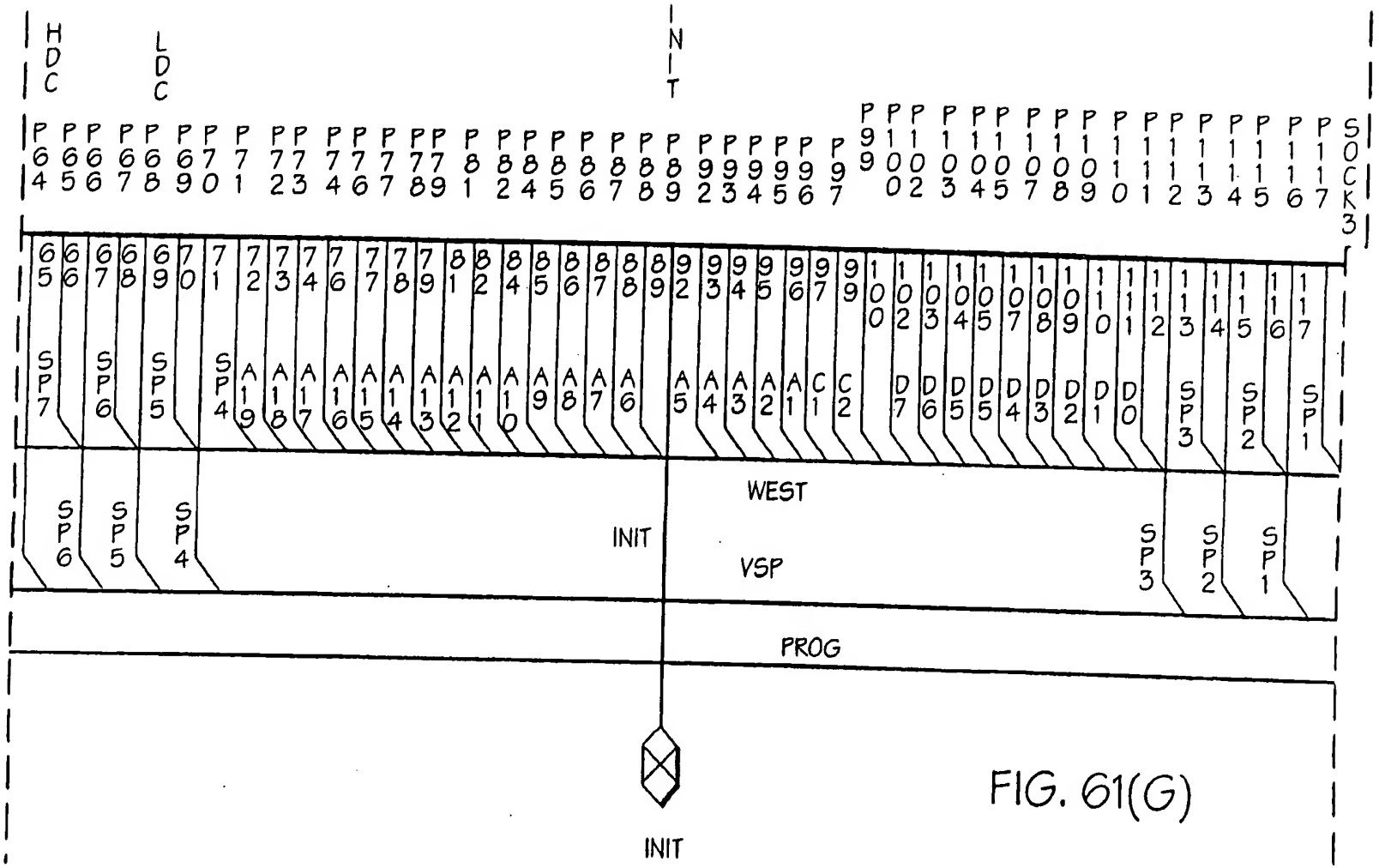


FIG. 61(G)

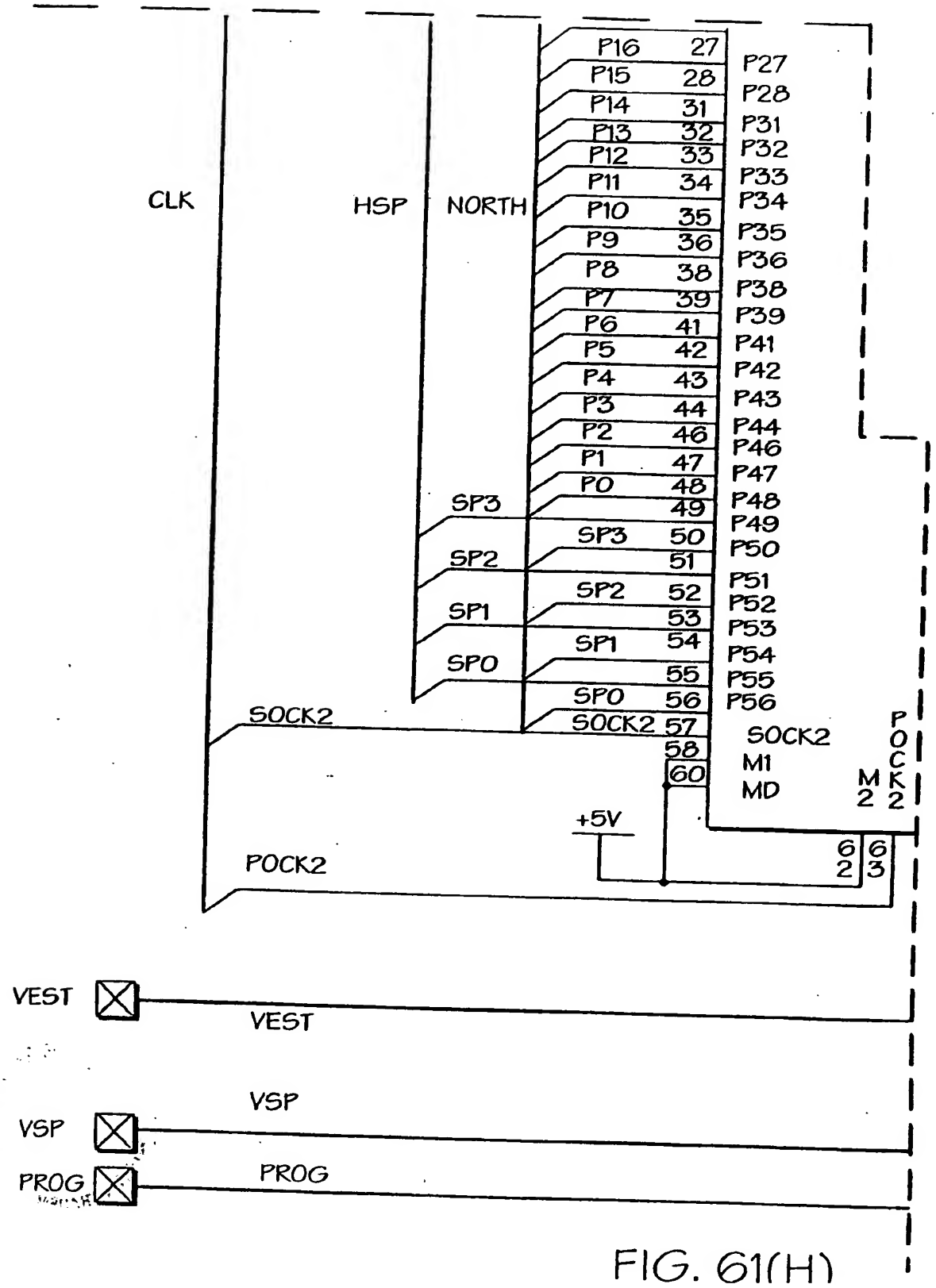

CLK
HSP
NORTH
P16 27
P15 28
P14 31
P13 32
P12 33
P11 34
P10 35
P9 36
P8 38
P7 39
P6 41
P5 42
P4 43
P3 44
P2 46
P1 47
P0 48
49
SP3
SP3 50
51
SP2
SP2 52
53
SP1
SP1 54
55
SP0
SP0 56
SOCK2 57
58
60
SOCK2
M1
MD
P27
P28
P31
P32
P33
P34
P35
P36
P38
P39
P41
P42
P43
P44
P46
P47
P48
P49
P50
P51
P52
P53
P54
P55
P56
SOCK2
POCK2
M2
+5V
62
63
POCK2
VEST
VEST
VSP
VSP
PROG
PROG

FIG. 61(H)

2014250 25802007

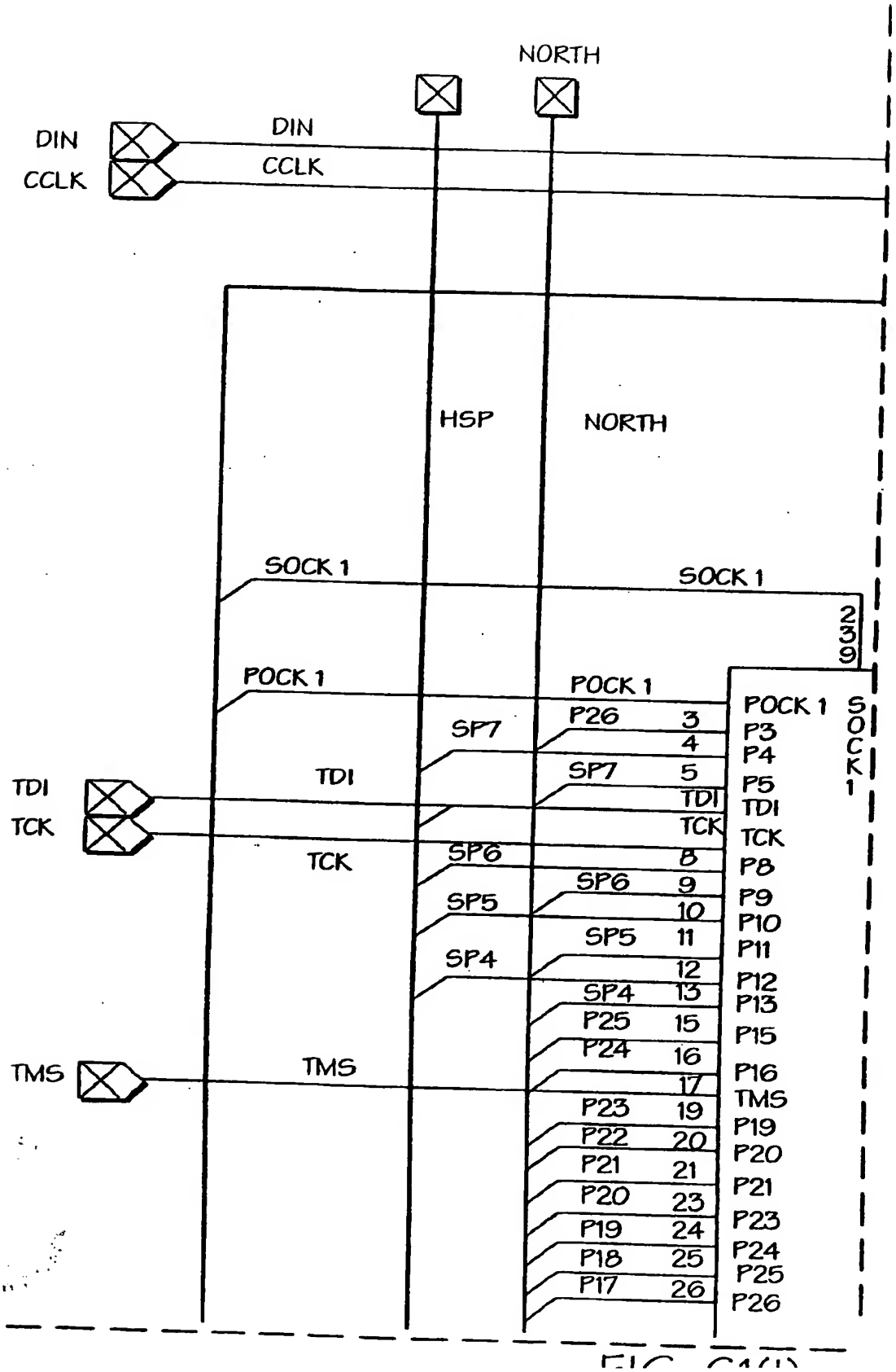


FIG. 6A(1)

DRAFT 20020807

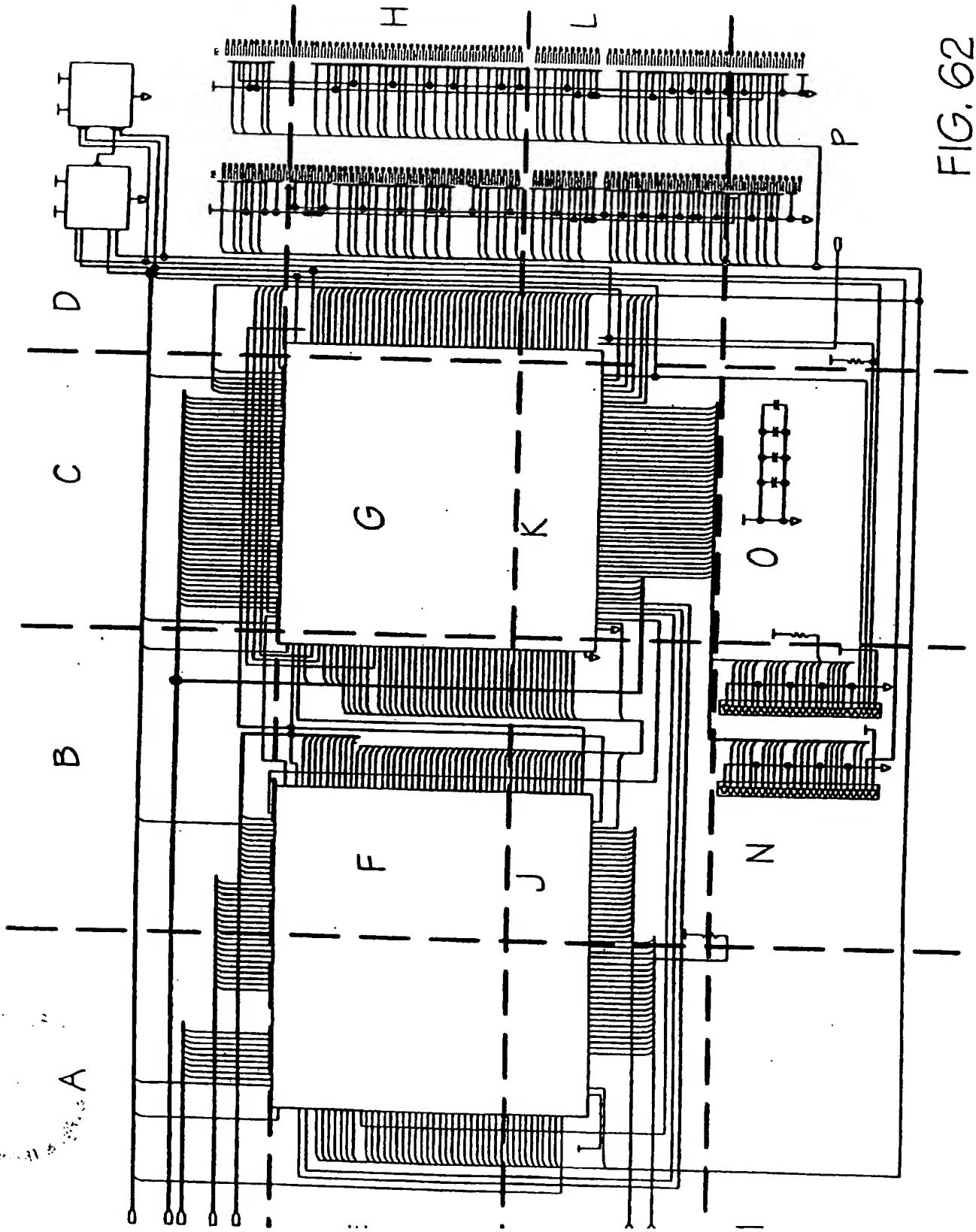
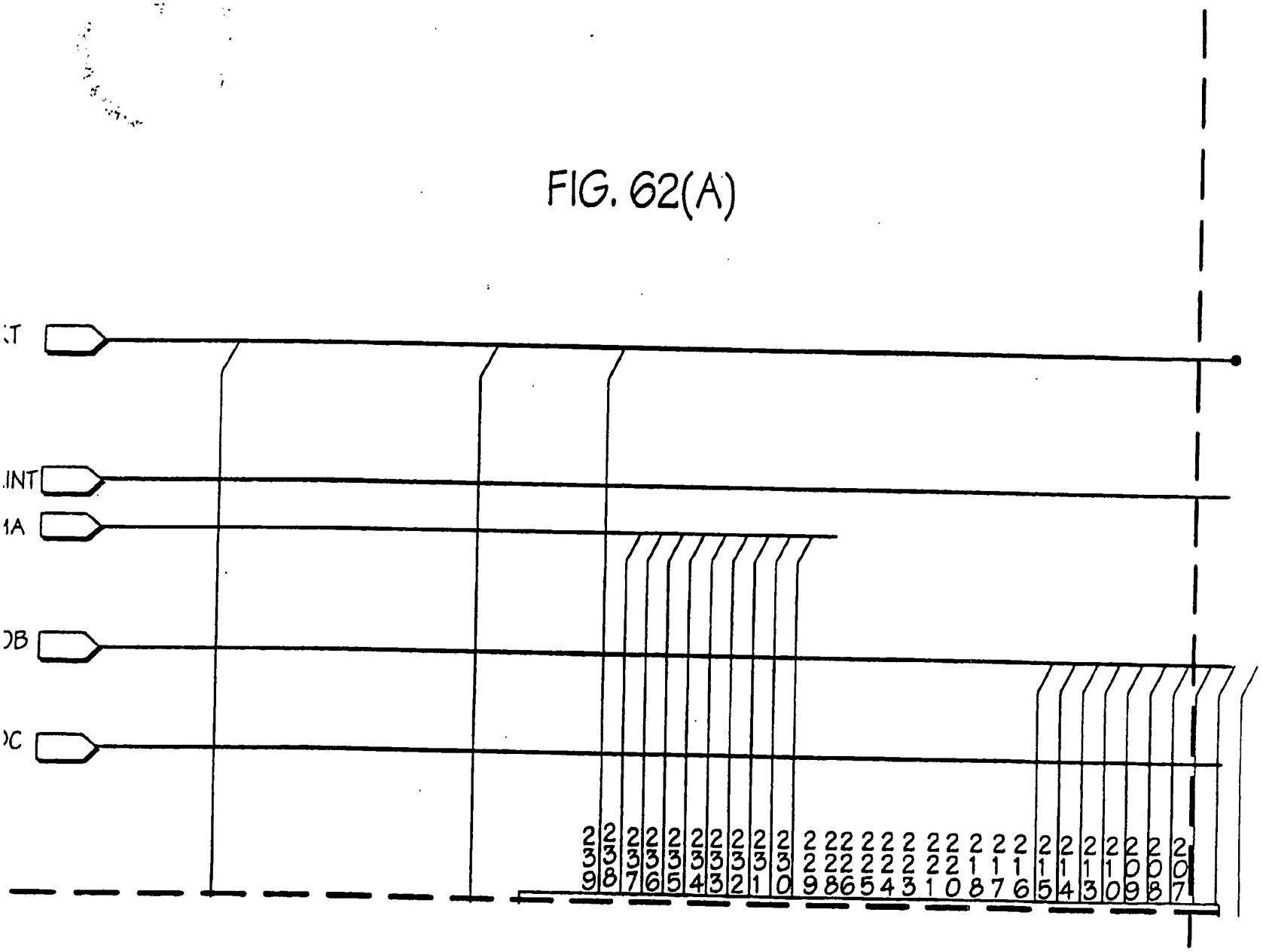


FIG. 62

FIG. 62(A)


:T
.INT
1A
)B
)C
2398
2387
2376
2365
2354
2343
2332
2321
2310
2298
2286
2265
2254
2243
2231
2208
2187
2176
2154
2143
2130
2109
2098
2087

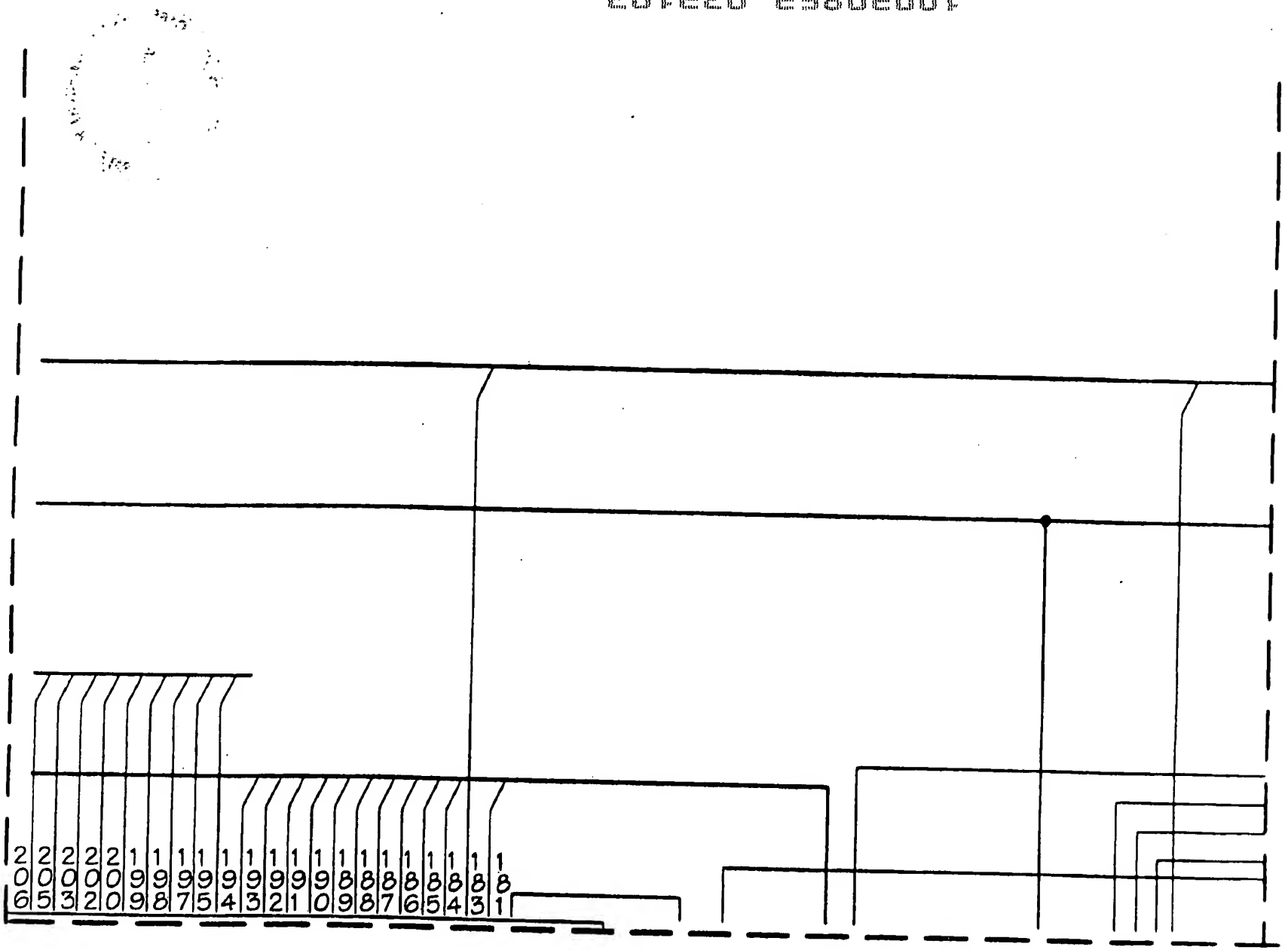

2006
2005
2003
2002
2000
1999
1998
1997
1995
1994
1993
1992
1991
1990
1989
1988
1987
1986
1985
1984
1983
1981

FIG. 62(B)

FIG. 62(C)

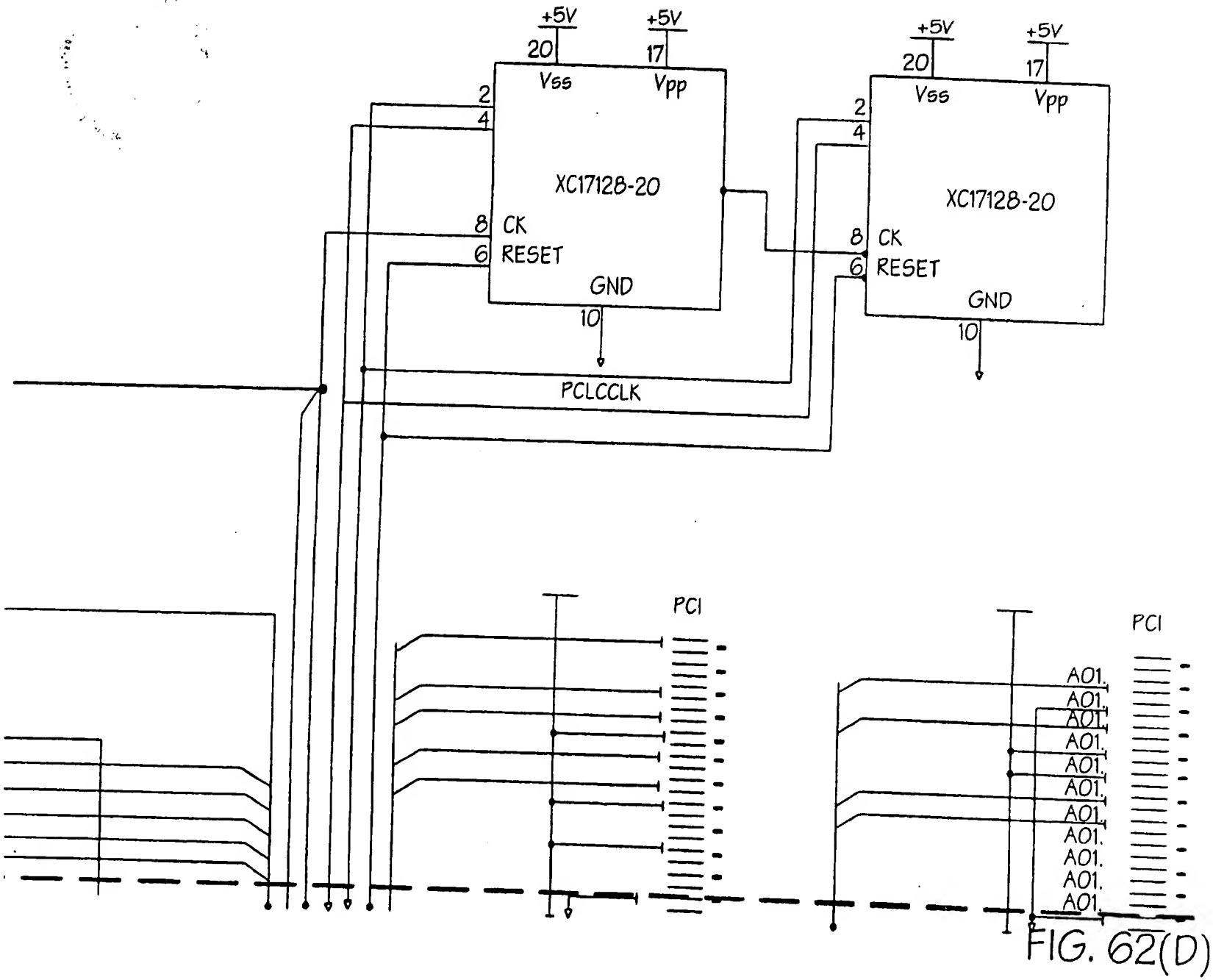
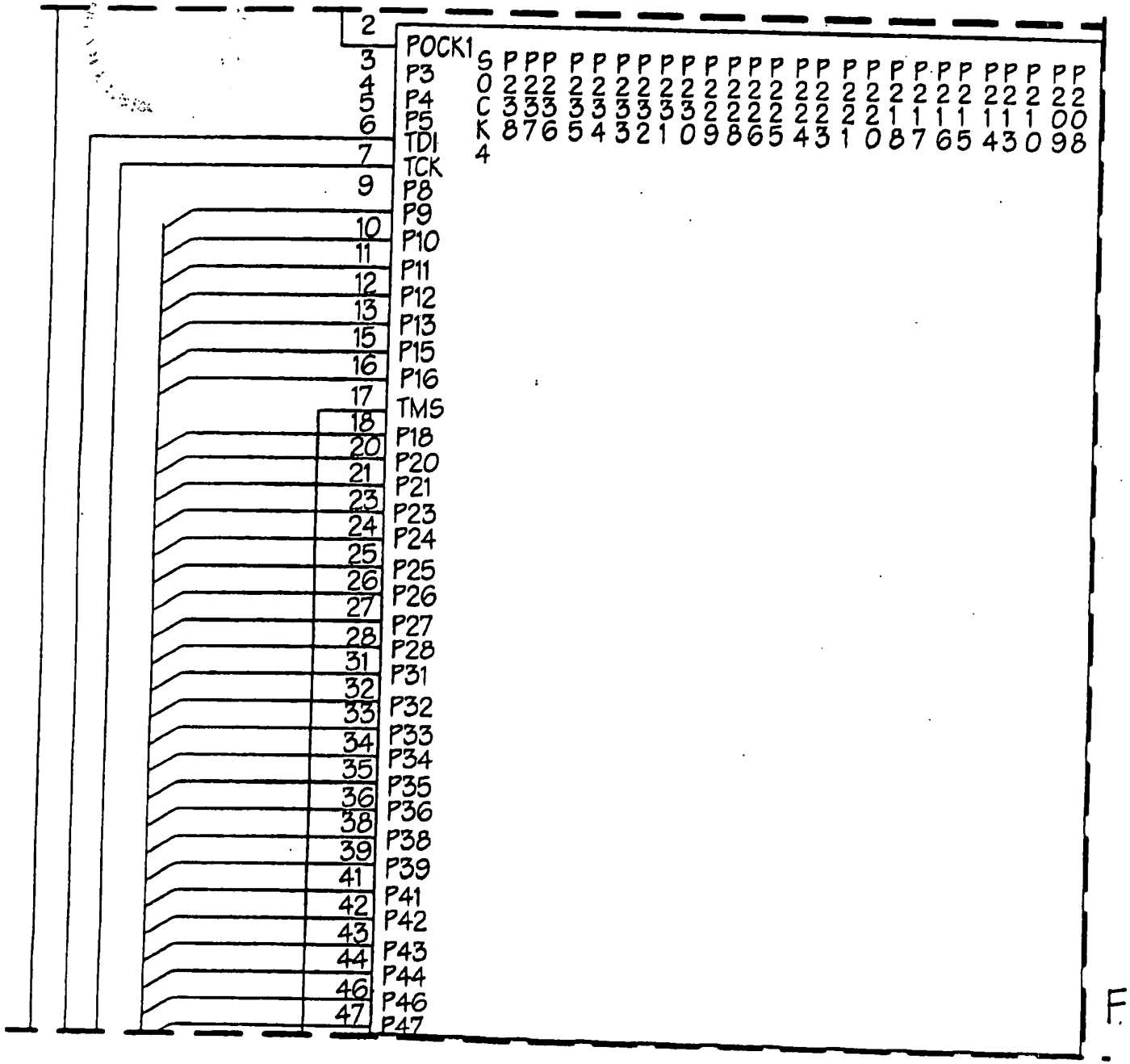

+5V
+5V
20
17
Vss
Vpp
2
4
XC17128-20
8
CK
6
RESET
GND
10
PCLCCLK
PCI
AO1.
AO1.
AO1.
AO1.
AO1.
AO1.
AO1.
AO1.
AO1.
AO1.

FIG. 62(D)


2
POCK1
3
P3
4
P4
5
P5
6
TDI
7
TCK
9
P8
10
P9
11
P10
12
P11
13
P12
15
P13
16
P15
17
P16
18
TMS
20
P18
21
P20
23
P21
24
P23
25
P24
26
P25
27
P26
28
P27
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P28
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P31
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P32
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P33
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P34
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P35
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P36
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P38
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P39
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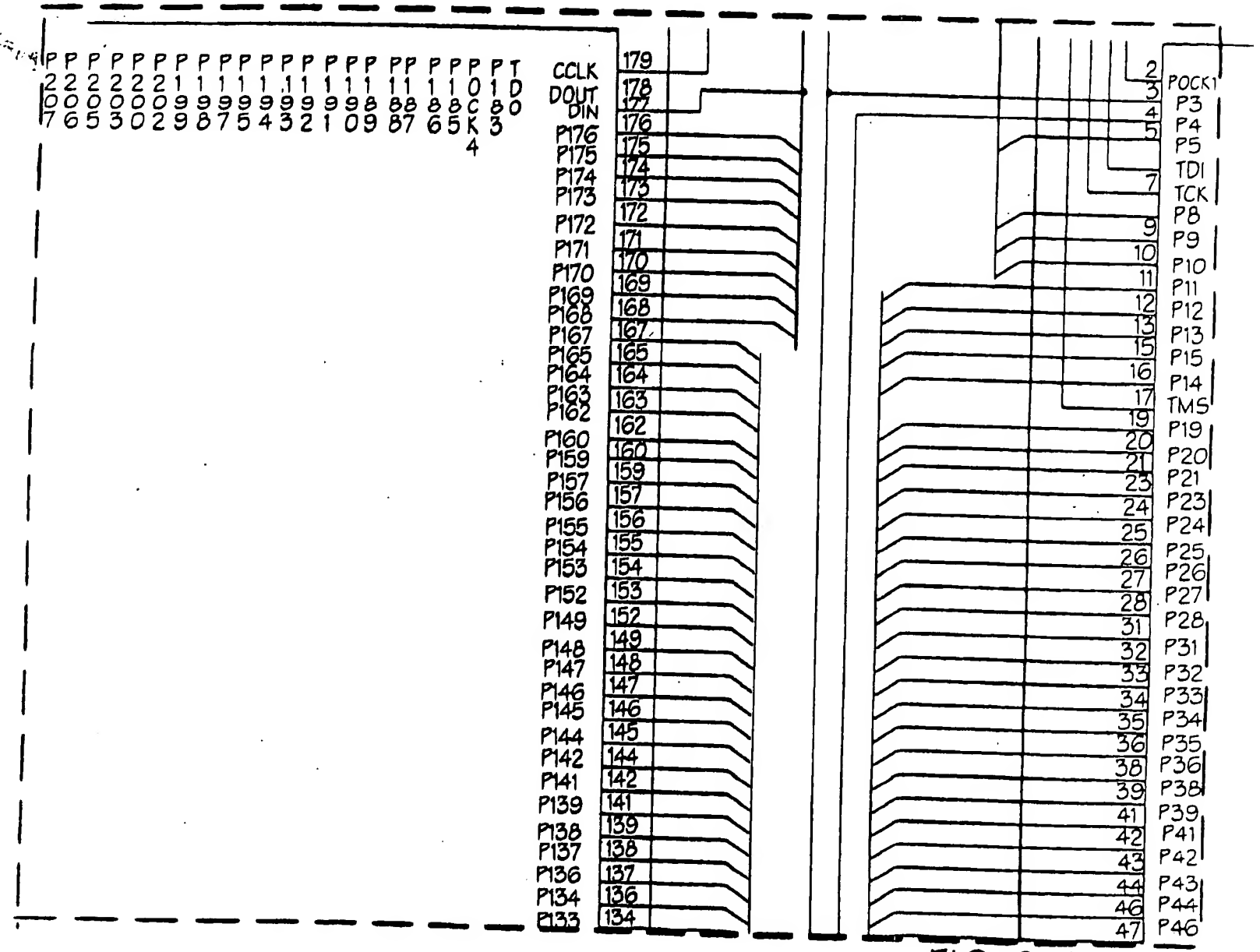
P41
43
P42
44
P43
46
P44
47
P46
P47
SOCK4
P2387
P2376
P2354
P2343
P2321
P2310
P2298
P2265
P2243
P2231
P2210
P2187
P2165
P2143
P2130
P2098

FIG. 62(E)


PP2007
PP2006
PP2005
PP2003
PP2002
PP2009
PP1998
PP1987
PP1975
PP1954
PP1943
PP1932
PP1921
PP1909
PP1898
PP1887
PP1876
PP1865
PP1854
PCK4
PP1843
TDO
CCLK
DOUT
DIN
P176
P175
P174
P173
P172
P171
P170
P169
P168
P167
P165
P164
P163
P162
P160
P159
P157
P156
P155
P154
P153
P152
P149
P148
P147
P146
P145
P144
P142
P141
P139
P138
P137
P136
P134
P133
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136
134
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24
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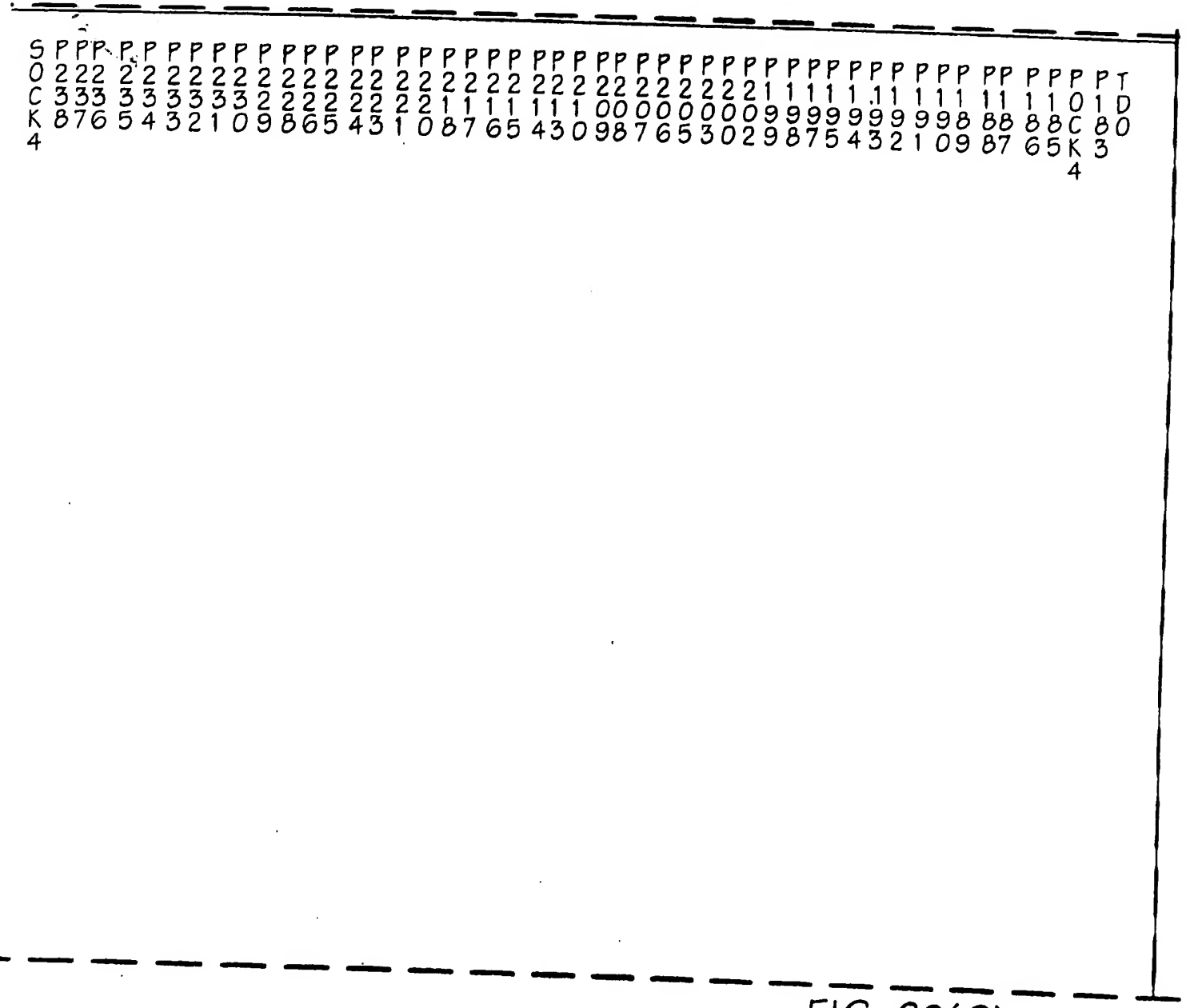
28
31
32
33
34
35
36
38
39
41
42
43
44
46
47
POCK1
P3
P4
P5
TDI
TCK
P8
P9
P10
P11
P12
P13
P15
P14
TMS
P19
P20
P21
P23
P24
P25
P26
P27
P28
P31
P32
P33
P34
P35
P36
P38
P39
P41
P42
P43
P44
P46

FIG. 62(F)

20120 "29802001


SOCK4
PP2233876
PP2233654
PP2233321
PP2233210
PP2222986
PP2222865
PP2222431
PP2222108
PP2221765
PP2221143
PP2221100
PP2220987
PP2220653
PP2220298
PP2211999
PP2211999
PP2211999

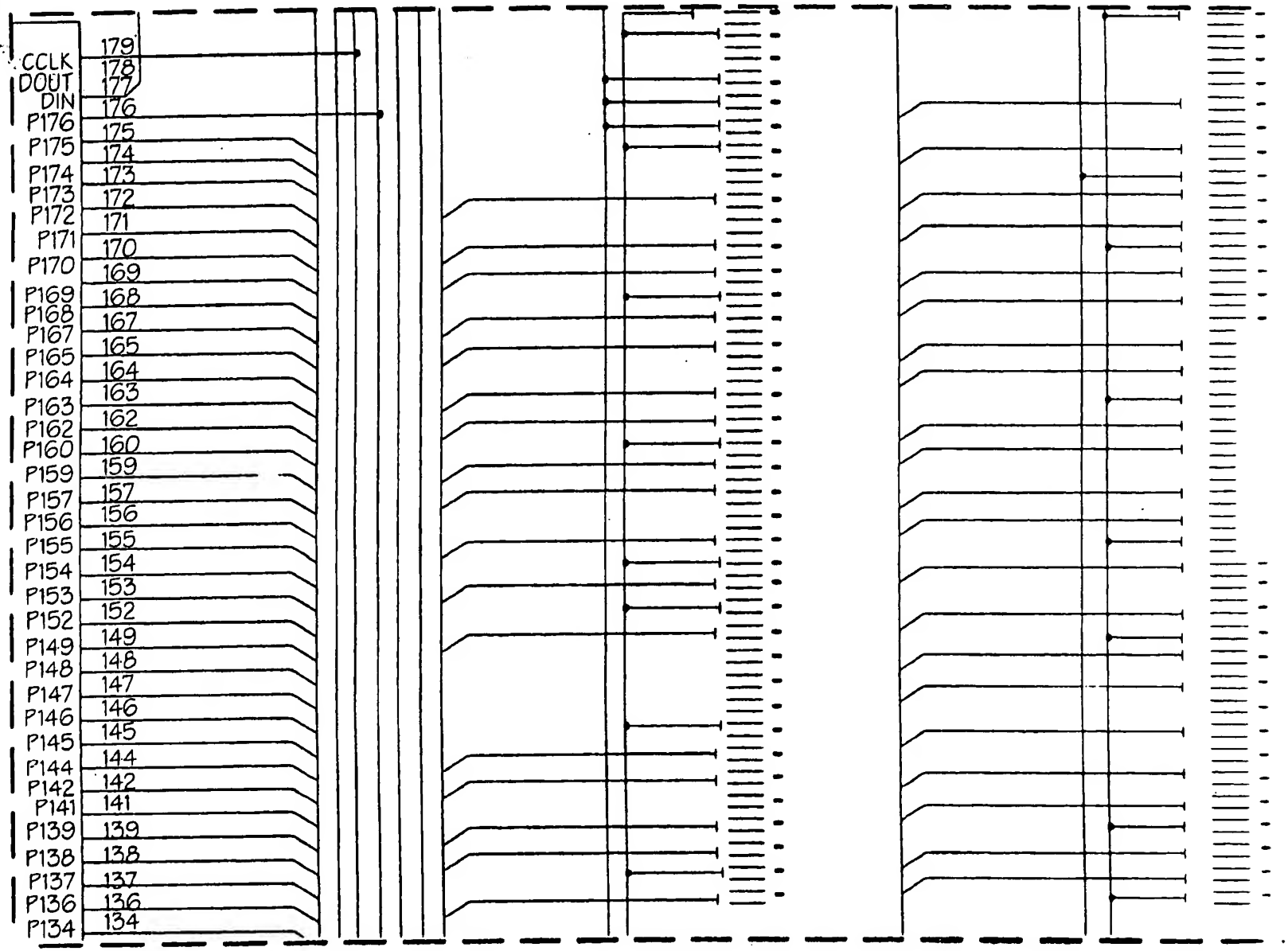
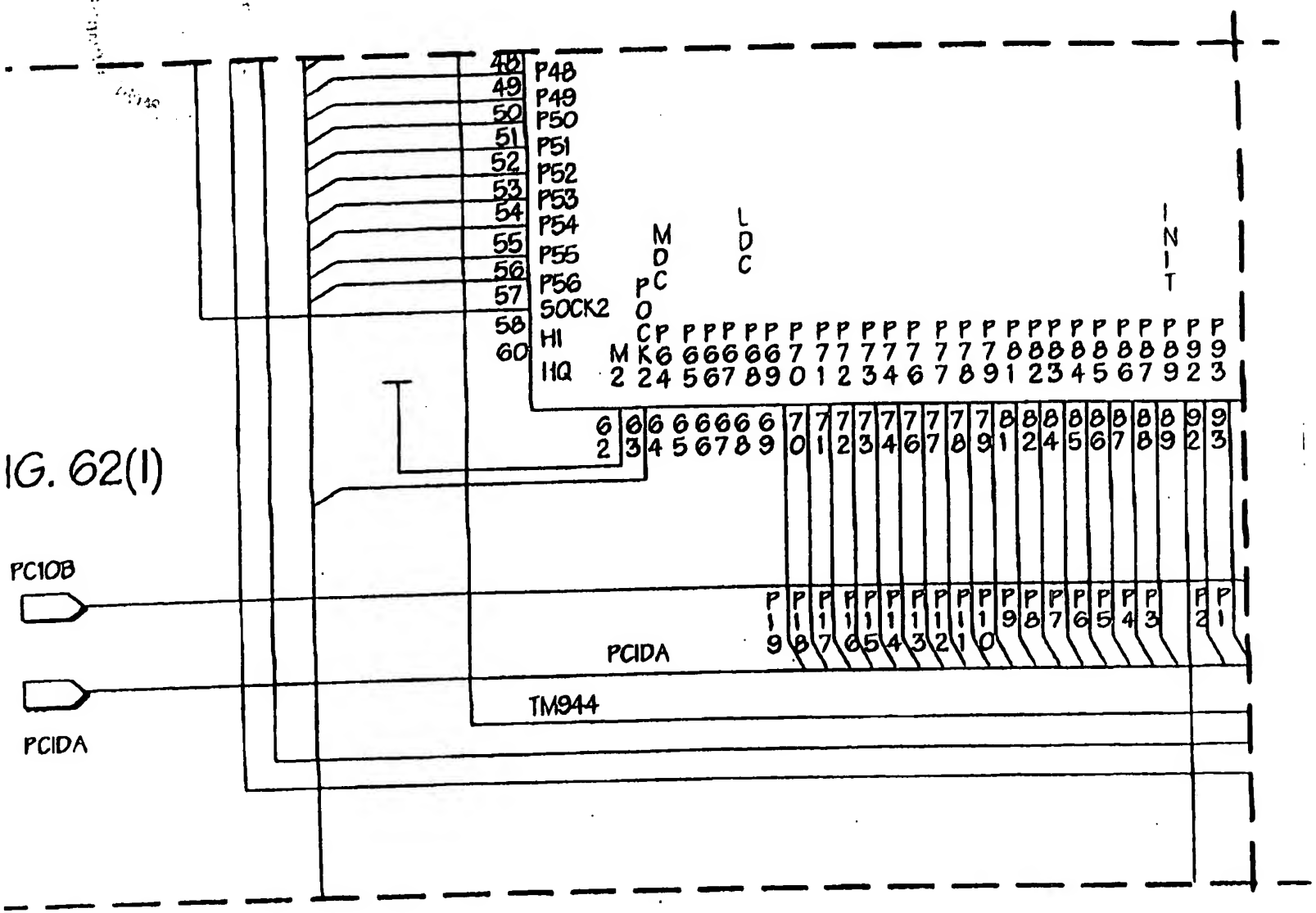

CCLK 179
DOUT 178
DIN 177
P176 176
P175 175
P174 174
P173 173
P172 172
P171 171
P170 170
P169 169
P168 168
P167 167
P165 165
P164 164
P163 163
P162 162
P160 160
P159 159
P157 157
P156 156
P155 155
P154 154
P153 153
P152 152
P149 149
P148 148
P147 147
P146 146
P145 145
P144 144
P142 142
P141 141
P139 139
P138 138
P137 137
P136 136
P134 134

FIG. 62(H)


48 P48
49 P49
50 P50
51 P51
52 P52
53 P53
54 P54
55 P55
56 P56
57 SOCK2
58 HI
60 HIQ
MDC
LDC
INIT
PC10B
PCIDA
PCIDA
TM944

IG. 62(1)

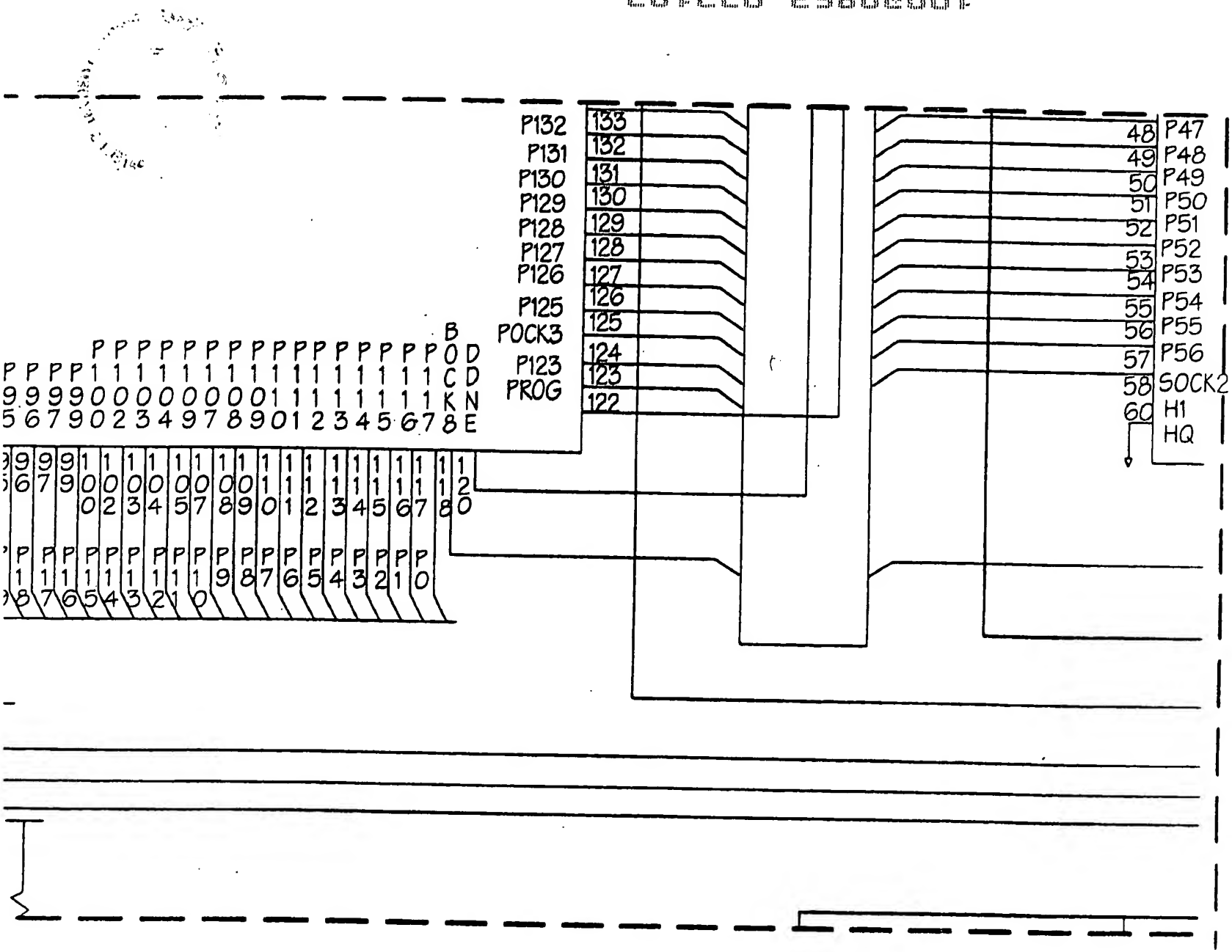

P132
P131
P130
P129
P128
P127
P126
P125
POCK3
P123
PROG
133
132
131
130
129
128
127
126
125
124
123
122
48 P47
49 P48
50 P49
51 P50
52 P51
52 P52
53 P53
54 P54
55 P55
56 P56
57 SOCK2
58 H1
60 HQ
P P P P P P P P P P P P P P P P P P P B D
9 9 9 9 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 O D
5 6 7 9 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 C N
0 2 3 4 5 7 8 9 0 1 2 3 4 5 6 7 K E
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2
0 2 3 4 5 7 8 9 0 1 2 3 4 5 6 7 8 0
P P P P P P P P P P P P P P P P P P P
1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0
8 7 6 5 4 3 2 1 0

FIG. 62(J)

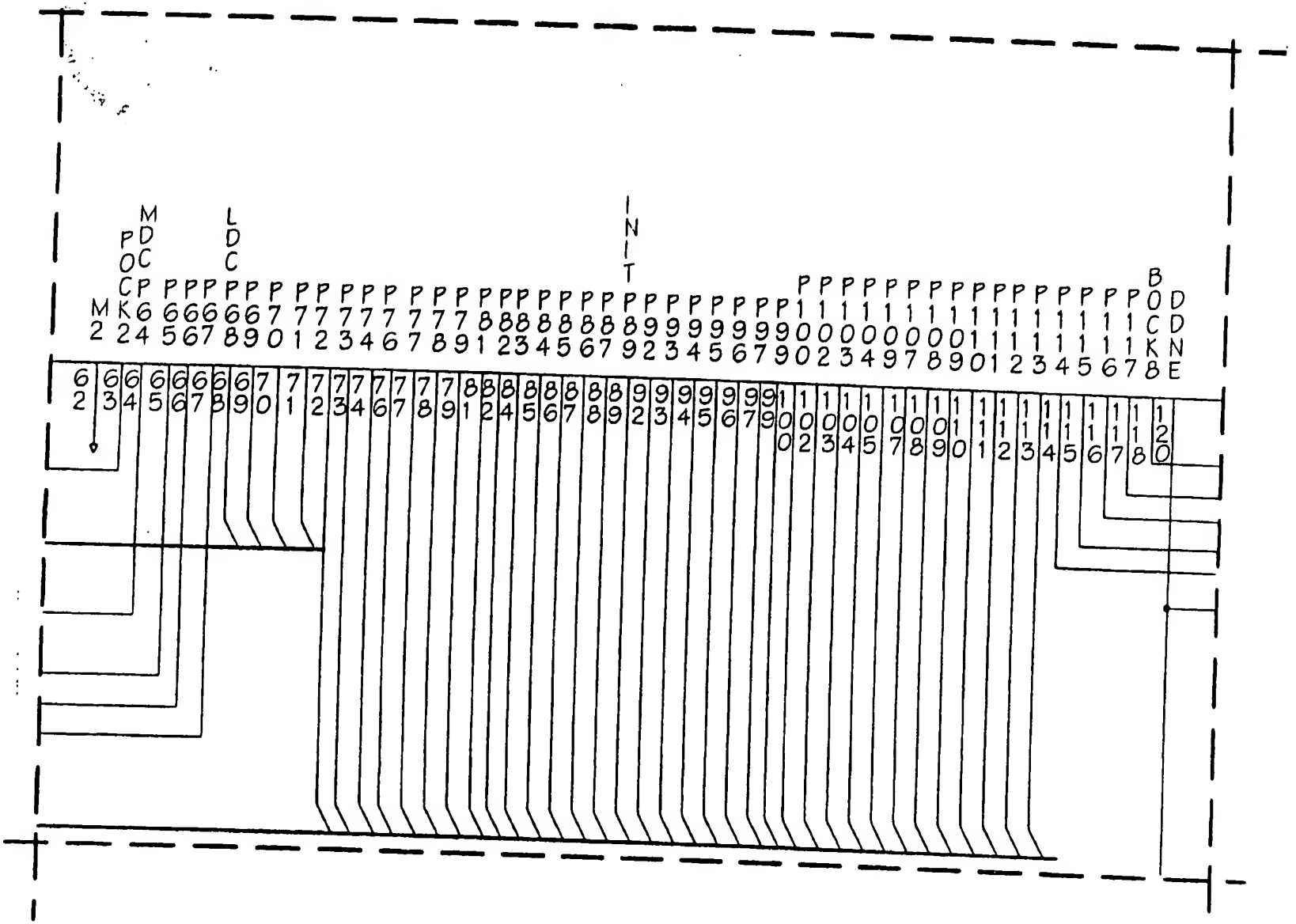

MDC
LDC
INIT
BOCK
DDNE
MK2
PPOCK624
PP6656
PP6667
PP6689
PP7701
PP7712
PP7734
PP7767
PP7789
PP8812
PP8834
PP8856
PP8878
PP8892
PP9923
PP9945
PP9967
PP9990
PP11002
PP11034
PP11056
PP11078
PP11090
PP11112
PP11134
PP11156
PP11178
PP11190
PP11212
PP11234
PP11256
PP11278
PP11290
BOCK8
DDNE
62 63 64 65 66 67 68 69 70 71 72 73 74 76 77 78 79 81 82 84 85 87 88 89 92 93 94 95 96 97 99 00 02 03 04 05 07 08 09 10 11 12 13 14 15 16 17 18 20

FIG. 62(K)

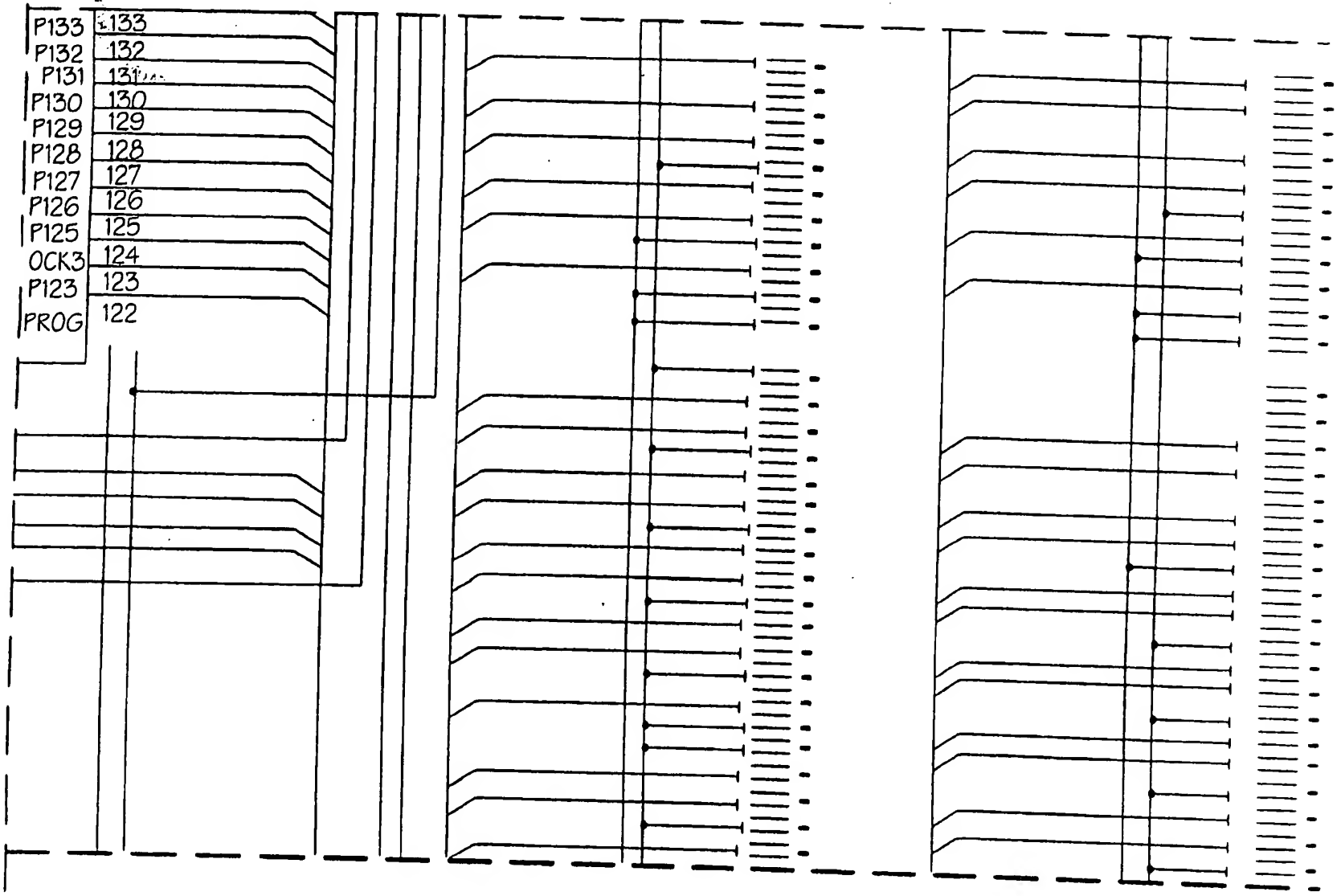

P133 133
P132 132
P131 131
P130 130
P129 129
P128 128
P127 127
P126 126
P125 125
OCK3 124
P123 123
PROG 122

FIG. 62(L)

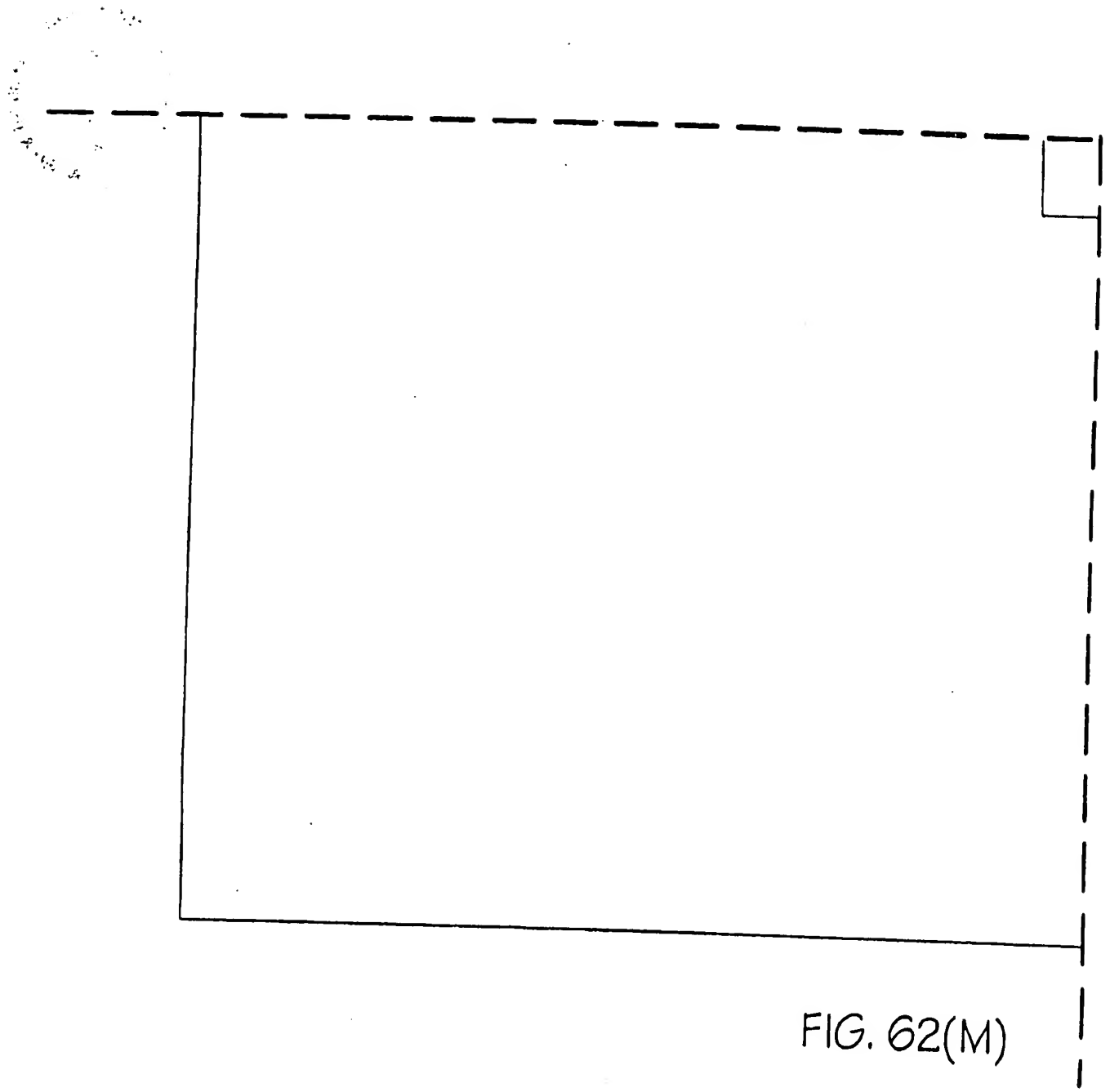
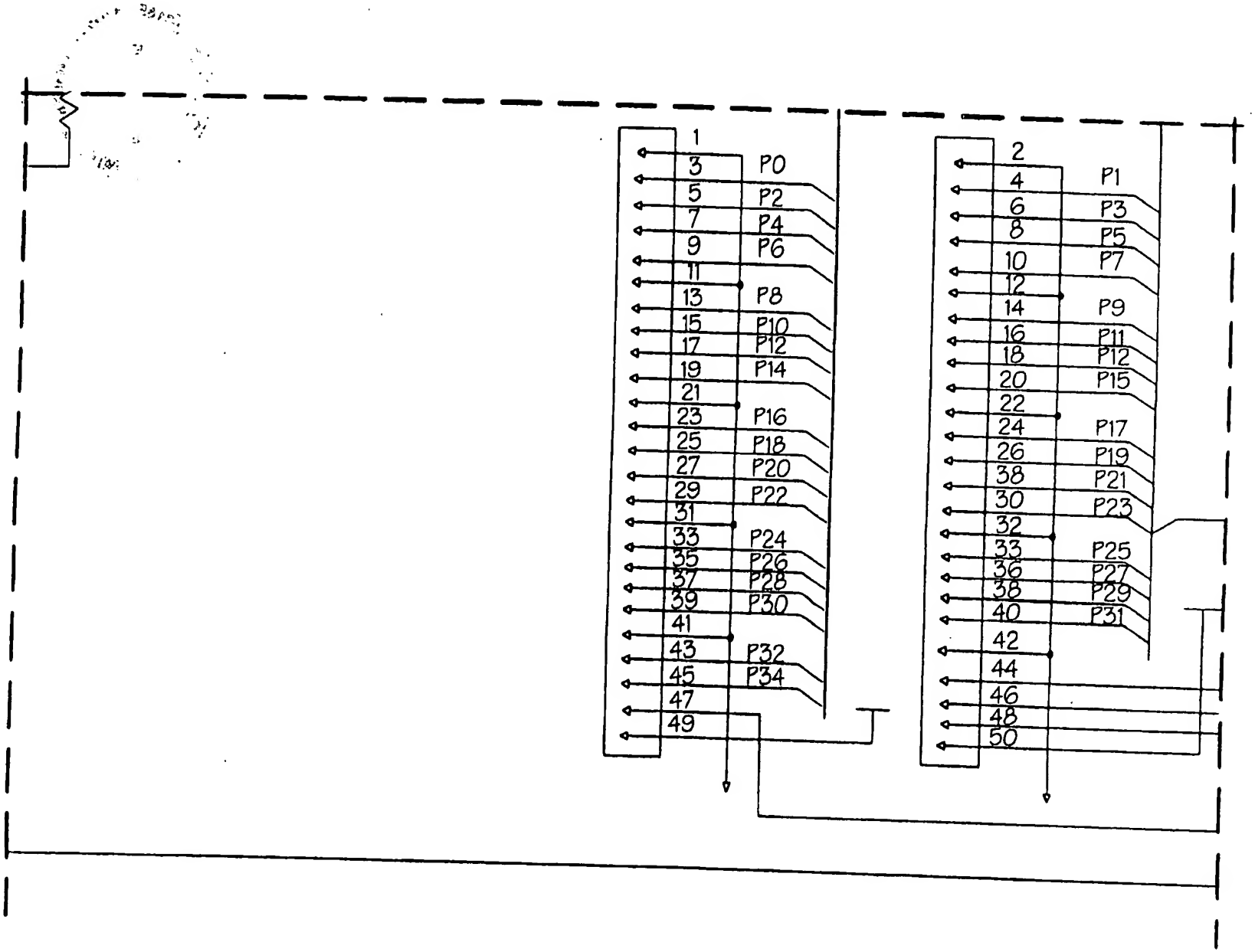


FIG. 62(M)


1
3
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9
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13
15
17
19
21
23
25
27
29
31
33
35
37
39
41
43
45
47
49
P0
P2
P4
P6
P8
P10
P12
P14
P16
P18
P20
P22
P24
P26
P28
P30
P32
P34
2
4
6
8
10
12
14
16
18
20
22
24
26
38
30
32
33
36
38
40
42
44
46
48
50
P1
P3
P5
P7
P9
P11
P12
P15
P17
P19
P21
P23
P25
P27
P29
P31

FIG. 62(N)

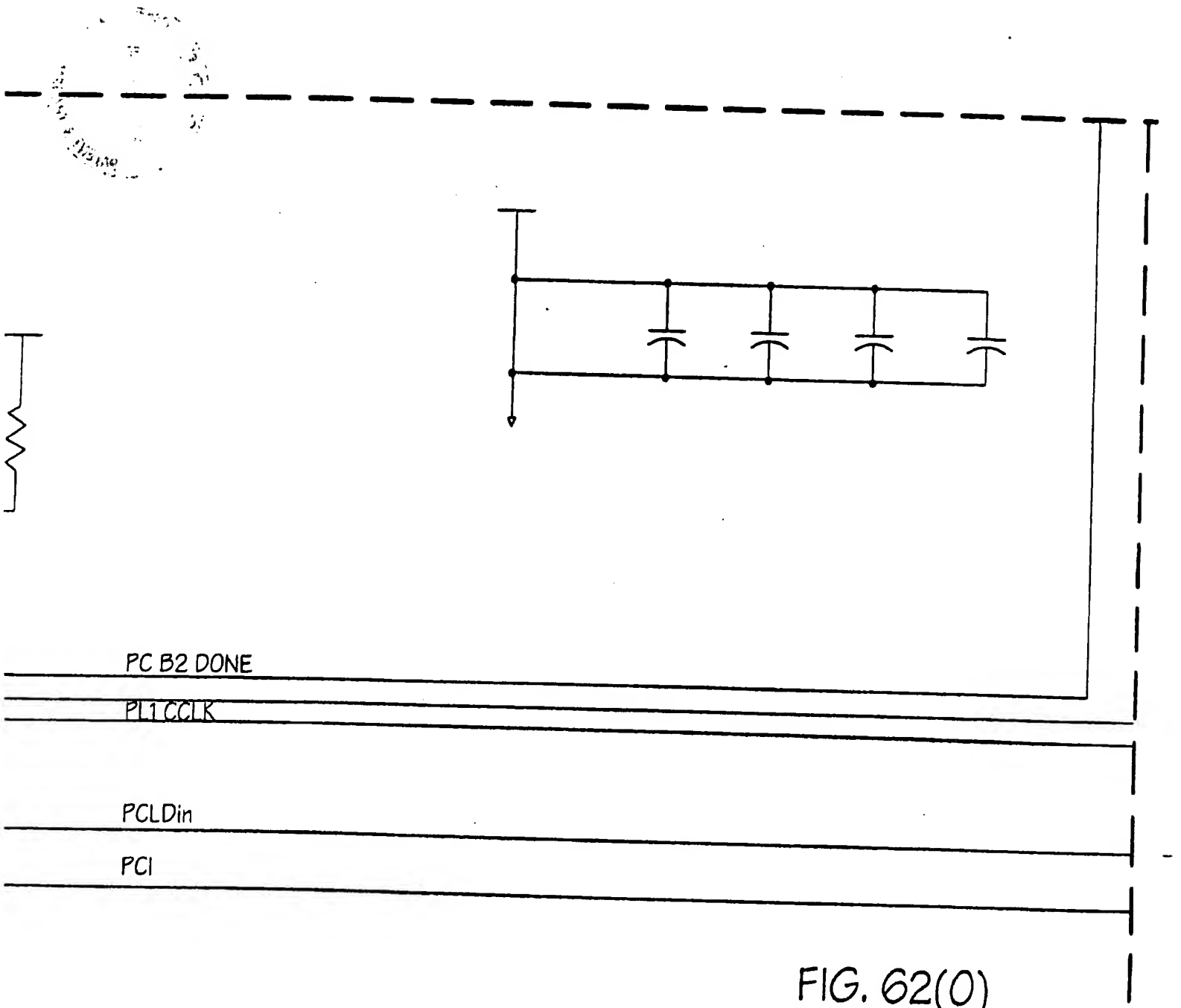


FIG. 62(0)

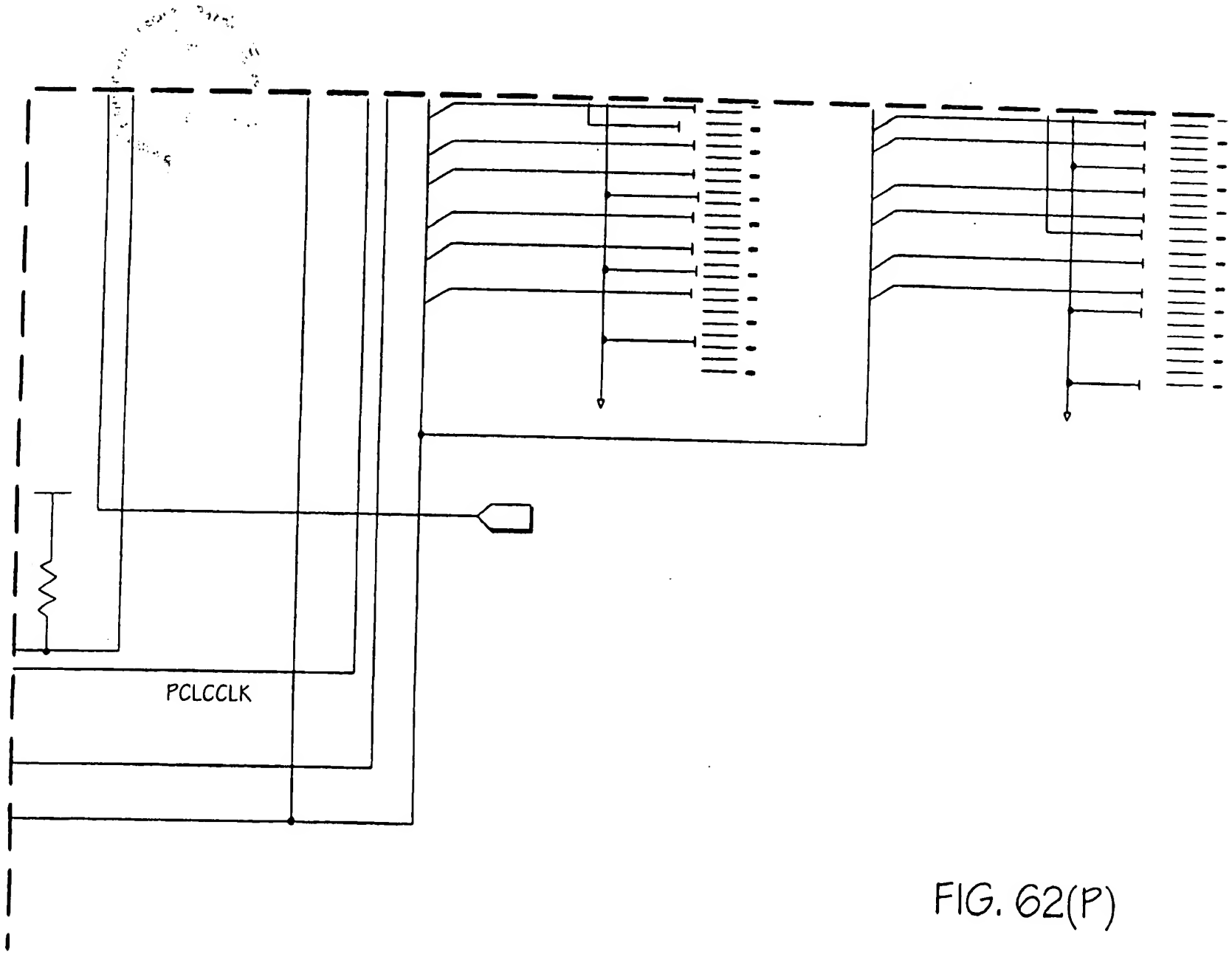


FIG. 62(P)

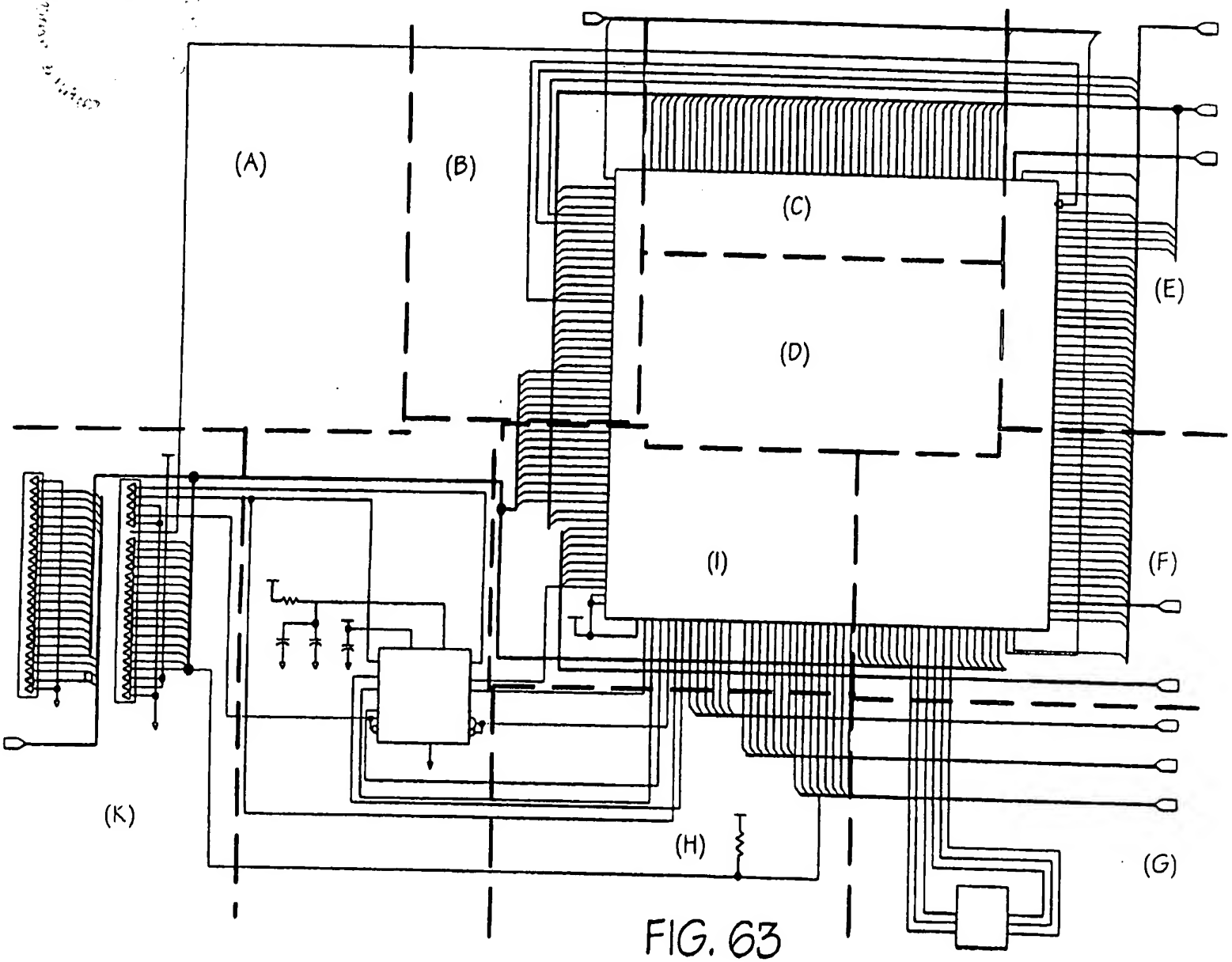


FIG. 63

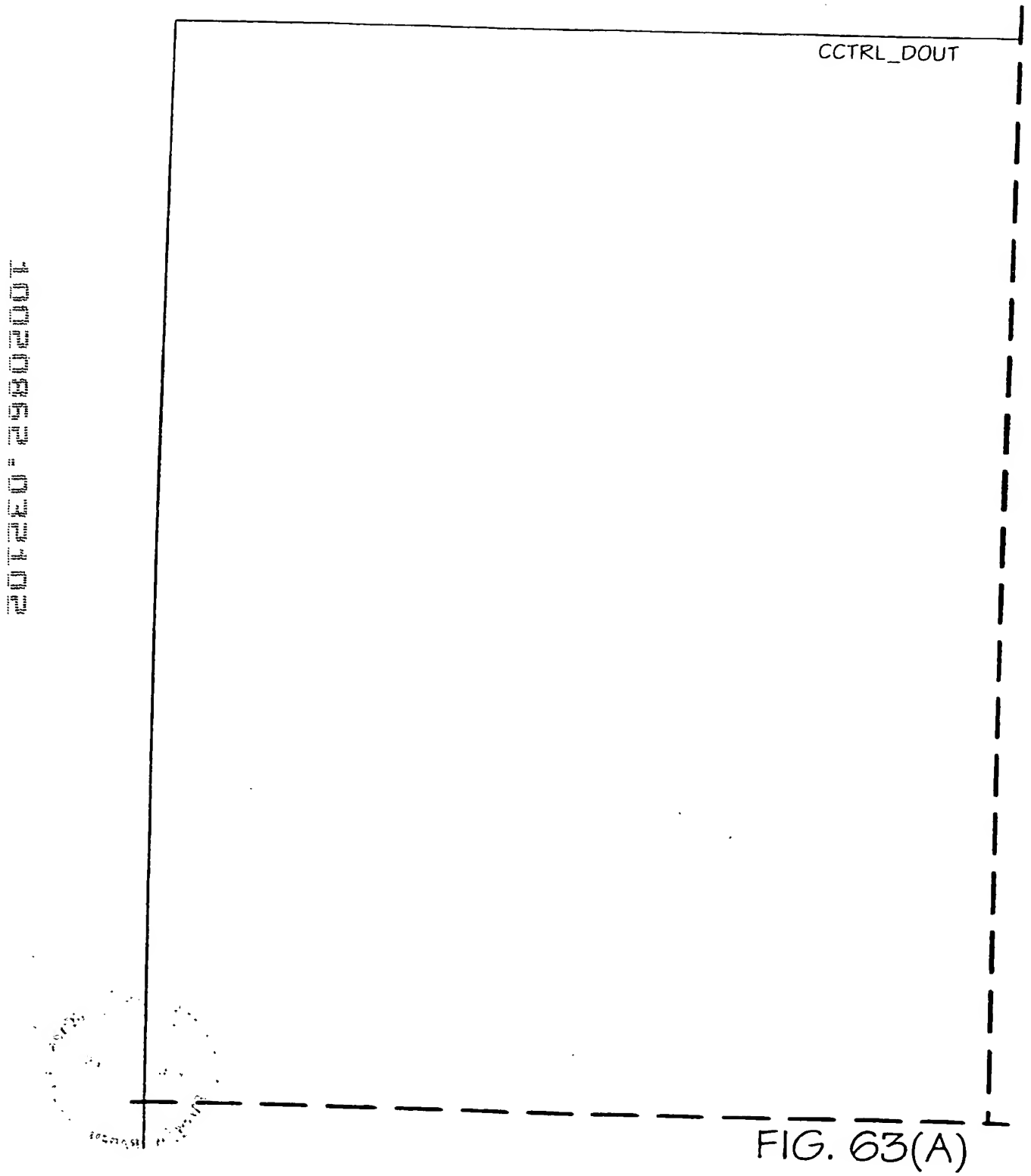


FIG. 63(A)

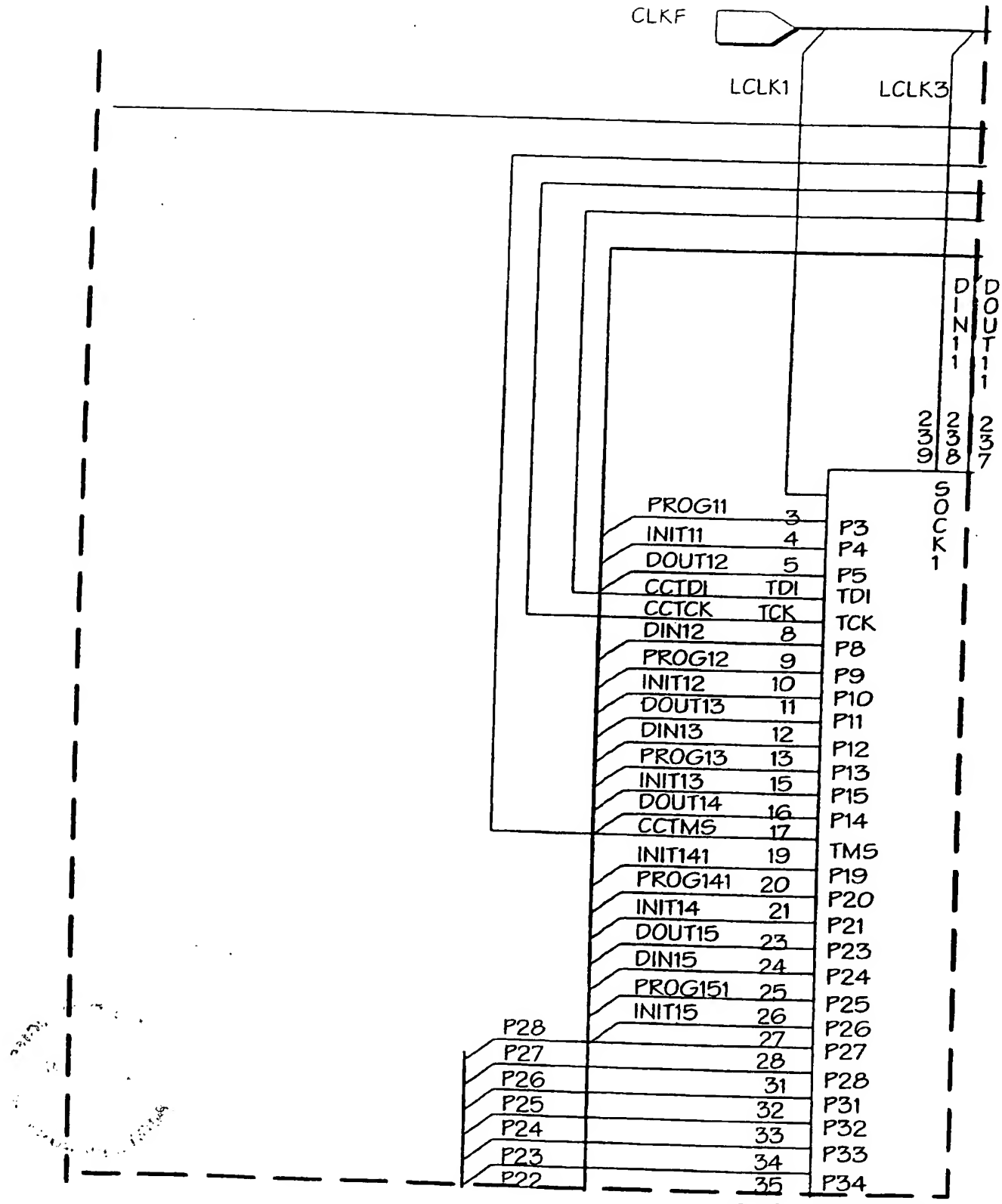

CLKF
LCLK1
LCLK3
DIN11
DOUT11
239
238
237
SOCK1
PROG11 3 P3
INIT11 4 P4
DOUT12 5 P5
CCTDI TDI TDI
CCTCK TCK TCK
DIN12 8 P8
PROG12 9 P9
INIT12 10 P10
DOUT13 11 P11
DIN13 12 P12
PROG13 13 P13
INIT13 15 P15
DOUT14 16 P14
CCTMS 17 TMS
INIT141 19 P19
PROG141 20 P20
INIT14 21 P21
DOUT15 23 P23
DIN15 24 P24
PROG151 25 P25
INIT15 26 P26
P28 27 P27
P27 28 P28
P26 31 P31
P25 32 P32
P24 33 P33
P23 34 P34
P22 35

FIG. 63(B)

20120-29802007

FIG. 63(C)

20T260" 29802007

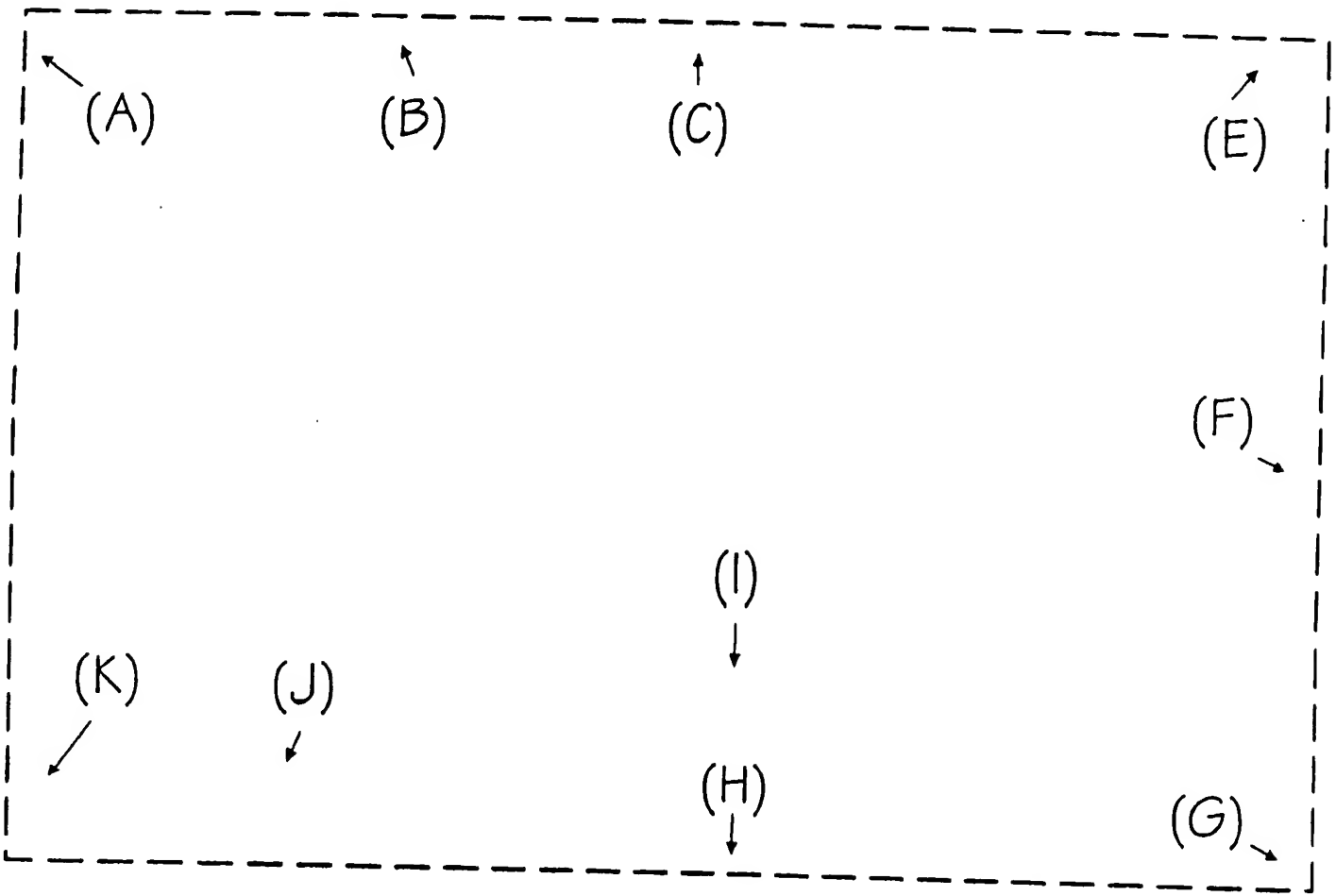


FIG. 63(D)

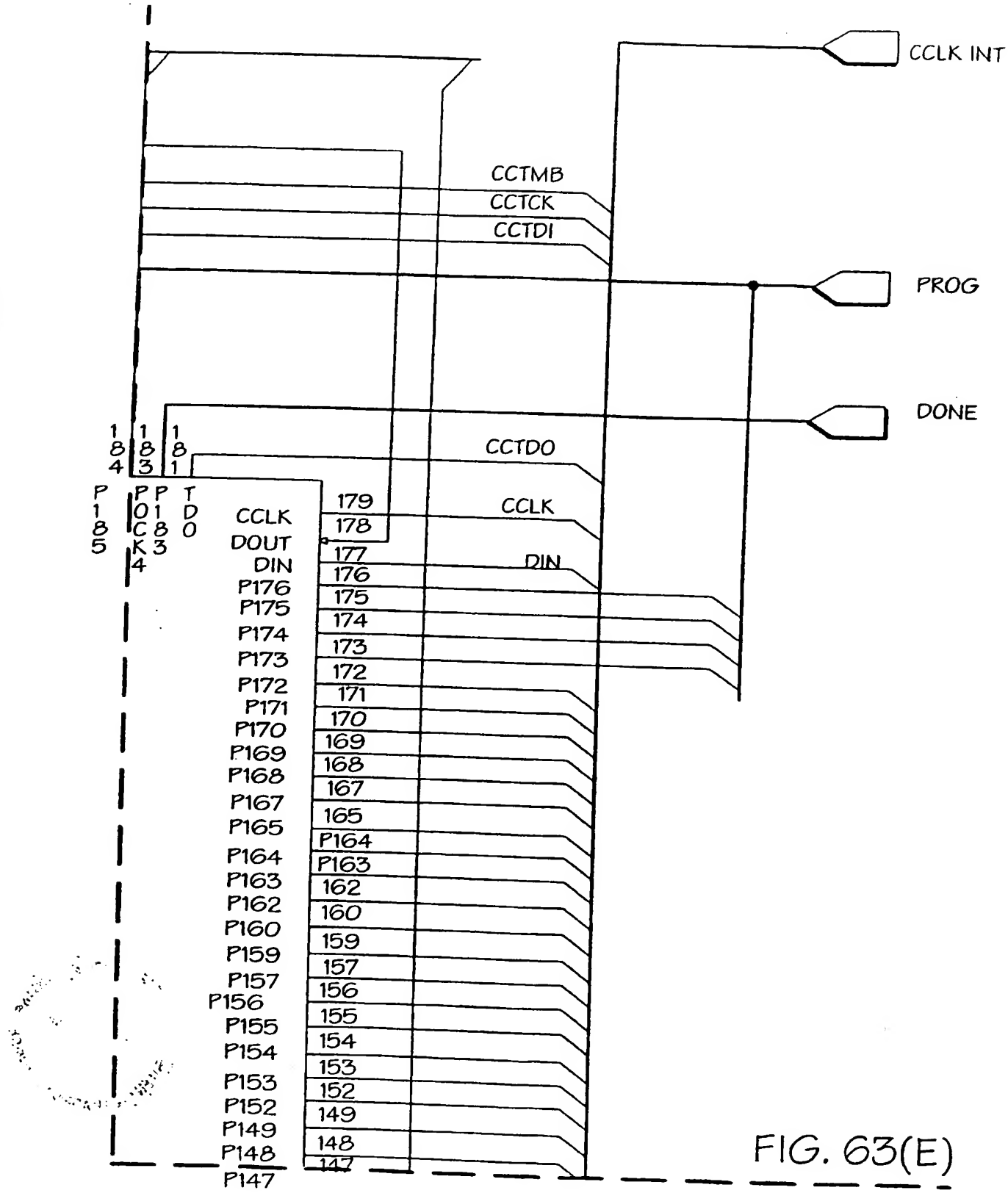

CCLK INT
CCTMB
CCTCK
CCTDI
PROG
DONE
CCTDO
CCLK
DIN
184
183
181
P185
PO1CK4
P183
TDO
CCLK
DOUT
DIN
P176
P175
P174
P173
P172
P171
P170
P169
P168
P167
P165
P164
P163
P162
P160
P159
P157
P156
P155
P154
P153
P152
P149
P148
P147
179
178
177
176
175
174
173
172
171
170
169
168
167
165
P164
P163
162
160
159
157
156
155
154
153
152
149
148
147

FIG. 63(E)

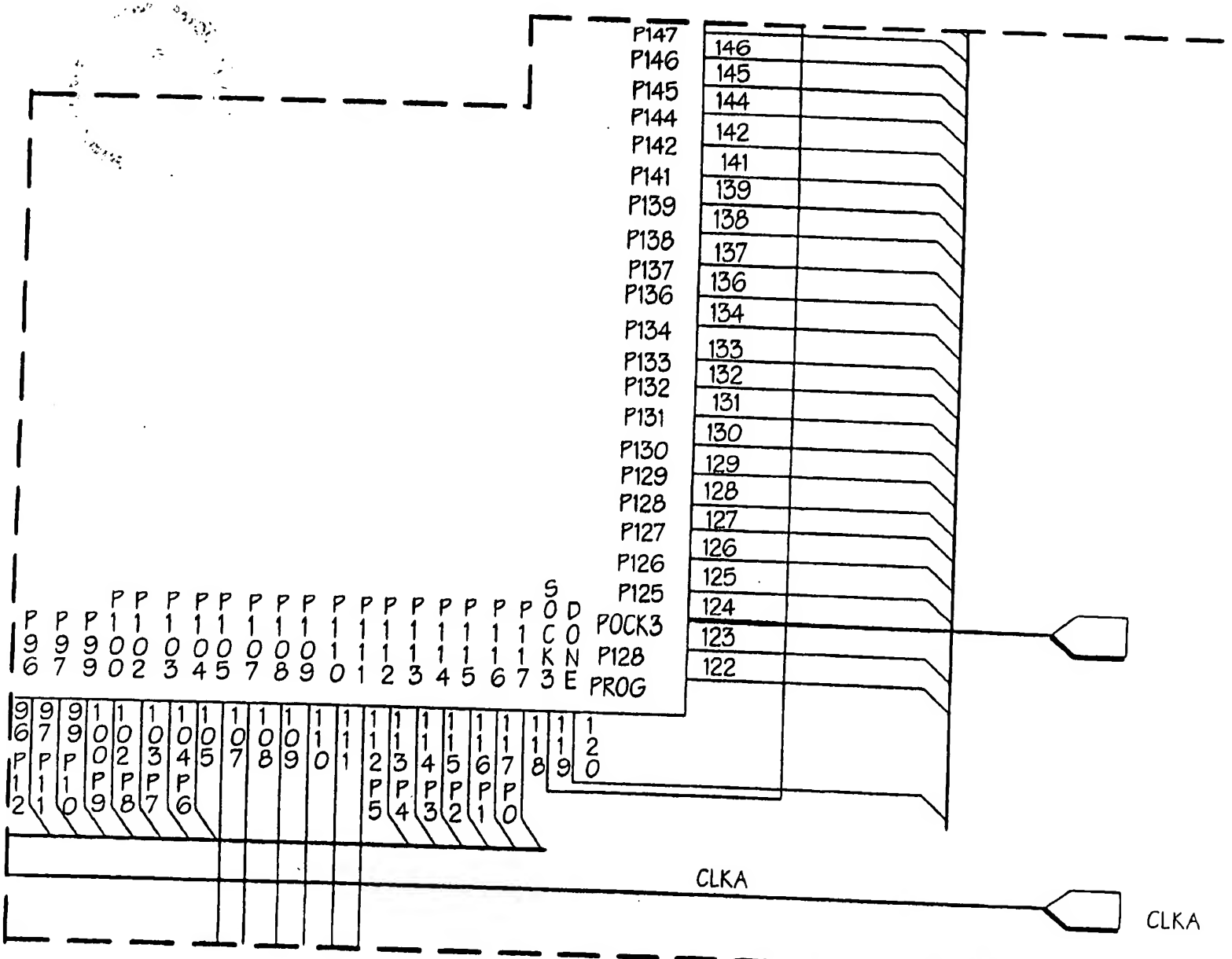

P147
P146
P145
P144
P142
P141
P139
P138
P137
P136
P134
P133
P132
P131
P130
P129
P128
P127
P126
P125
146
145
144
142
141
139
138
137
136
134
133
132
131
130
129
128
127
126
125
124
123
122
P96
P97
P99
P100
P102
P103
P104
P105
P107
P108
P109
P110
P111
P112
P113
P114
P115
P116
P117
SOCK3
DON E
POCK3
P128
PROG
96 P12
97 P11
99 P10
100 P9
102 P8
103 P7
104 P6
105
107
108
109
110
111
112 P5
113 P4
114 P3
115 P2
116 P1
117 P0
118
119
120
CLKA
CLKA

FIG. 63(F)

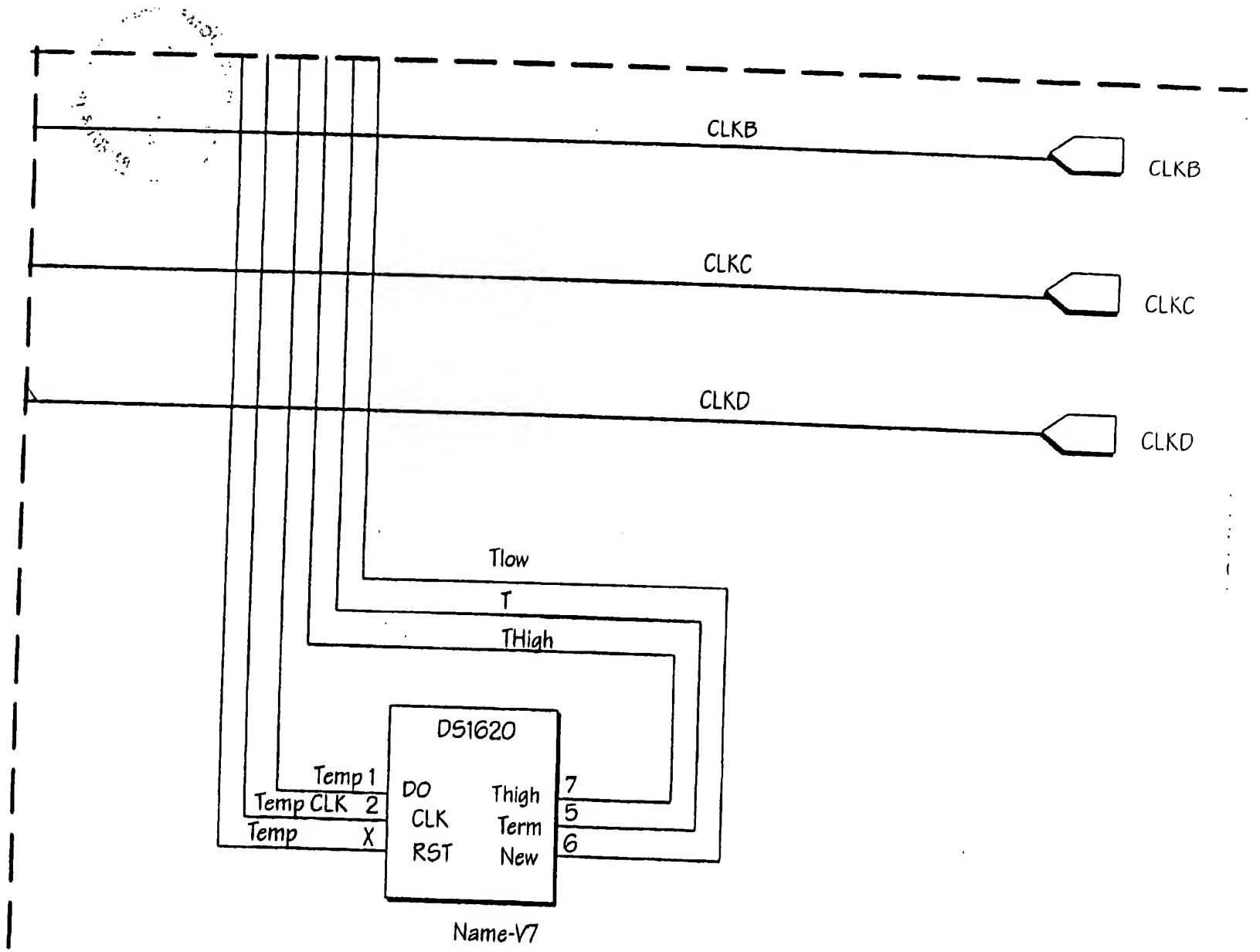

CLKB
CLKB
CLKC
CLKC
CLKD
CLKD
Tlow
T
THigh
DS1620
Temp 1
Temp CLK 2
Temp X
DO
CLK
RST
Thigh 7
Term 5
New 6
Name-V7

FIG. 63(G)

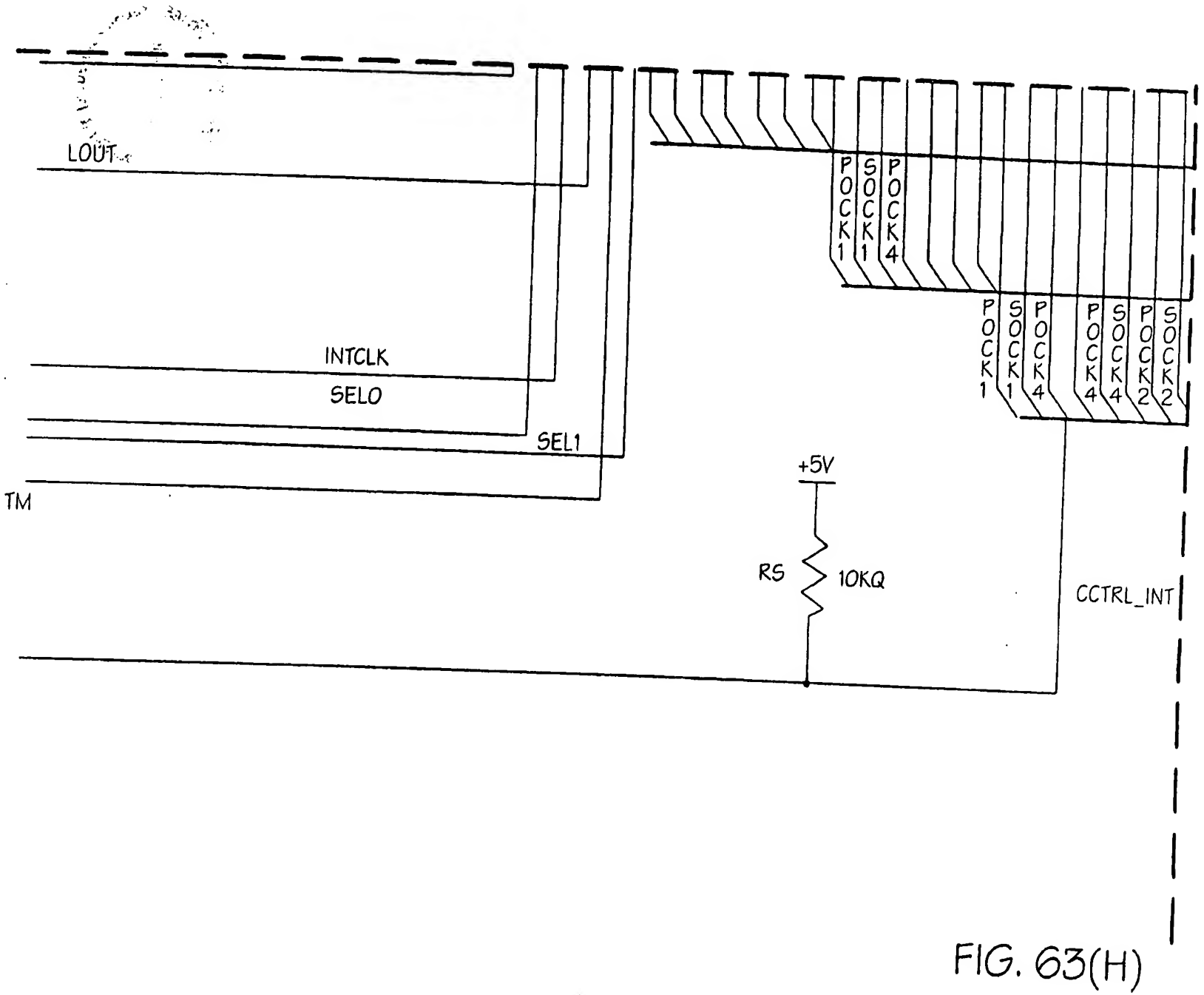

LOUT
INTCLK
SELO
SEL1
TM
+5V
RS
10KQ
CCTRL_INT
POCK1
SOCK1
POCK4
POCK1
SOCK1
POCK4
POCK4
SOCK4
POCK2
SOCK2

FIG. 63(H)

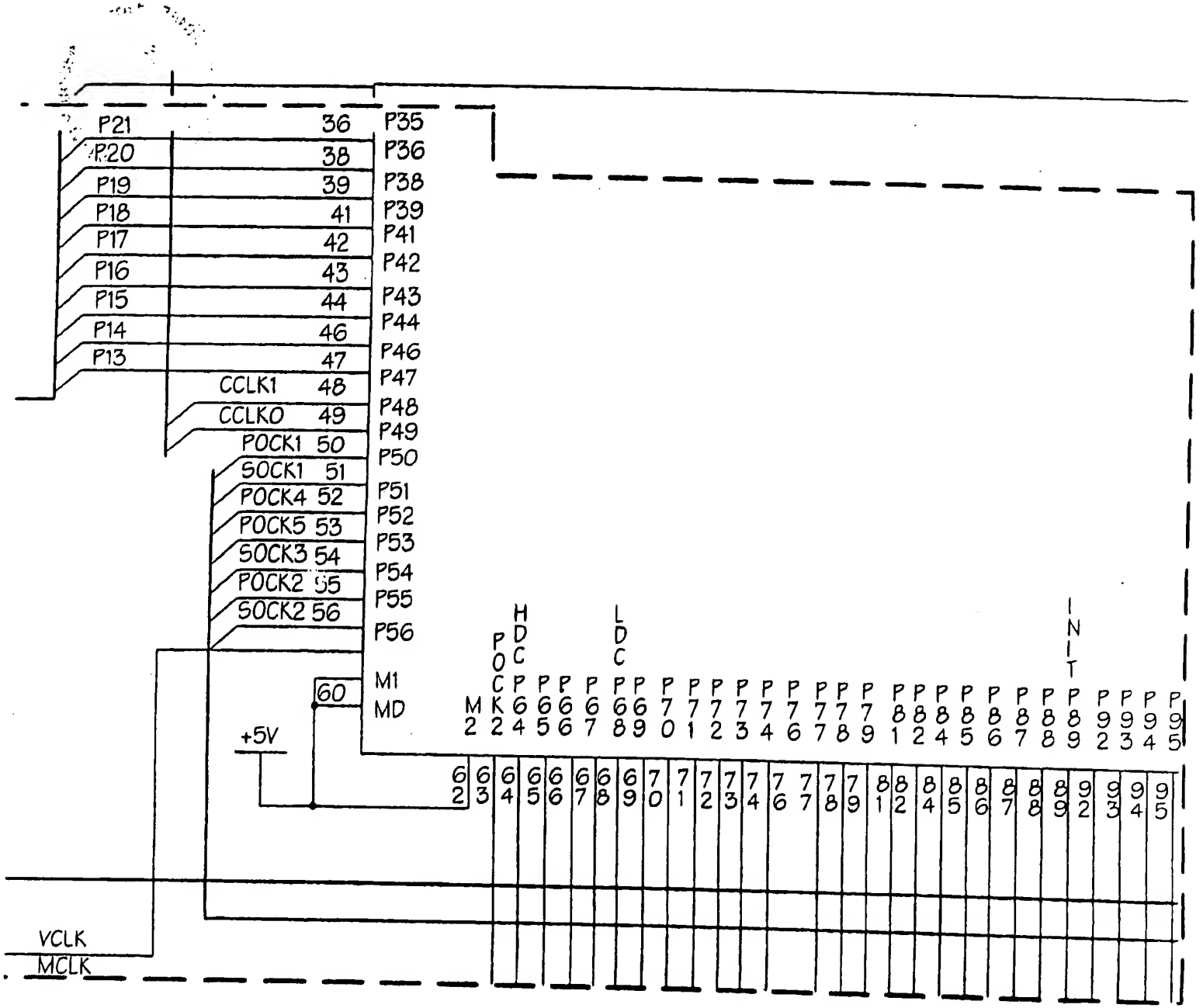
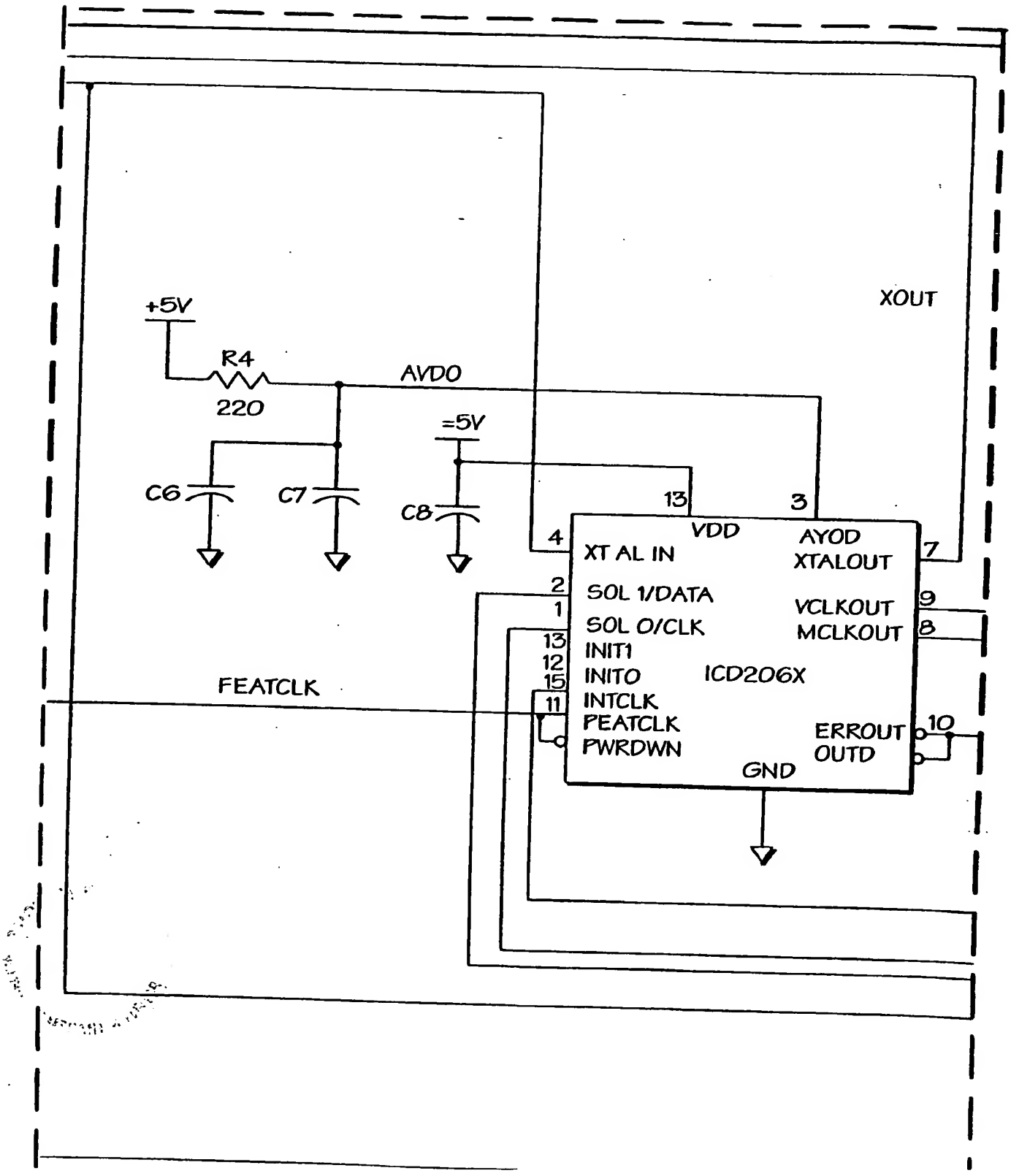

P21 36 P35
P20 38 P36
P19 39 P38
P18 41 P39
P17 42 P41
P16 43 P42
P15 44 P43
P14 46 P44
P13 47 P46
CCLK1 48 P47
CCLKO 49 P48
POCK1 50 P49
SOCK1 51 P50
POCK4 52 P51
POCK5 53 P52
SOCK3 54 P53
POCK2 55 P54
SOCK2 56 P55
P56
M1
60
MD
+5V
VCLK
MCLK
POCKM2
HDCP624
P625
P626
P627
LDCP628
P629
P630
P631
P632
P633
P634
P635
P636
P637
P638
P639
P641
P642
P643
P644
P646
P647
P648
P649
P650
P651
P652
P653
P654
P655
P656
INITP689
P692
P693
P694
P695
62 63 64 65 66 67 68 69 70 71 72 73 74 76 77 78 79 81 82 84 85 86 87 88 89 92 93 94 95

FIG. 63(1)


+5V
R4
220
AVDO
=5V
C6
C7
C8
XOUT
13
VDD
3
4
XT AL IN
AYOD
XTALOUT
7
2
SOL 1/DATA
1
SOL O/CLK
VCLKOUT
9
MCLKOUT
8
13
INIT1
12
INITO
15
INTCLK
11
PEATCLK
PWRDWN
ICD206X
FEATCLK
ERROUT
10
OUTD
GND

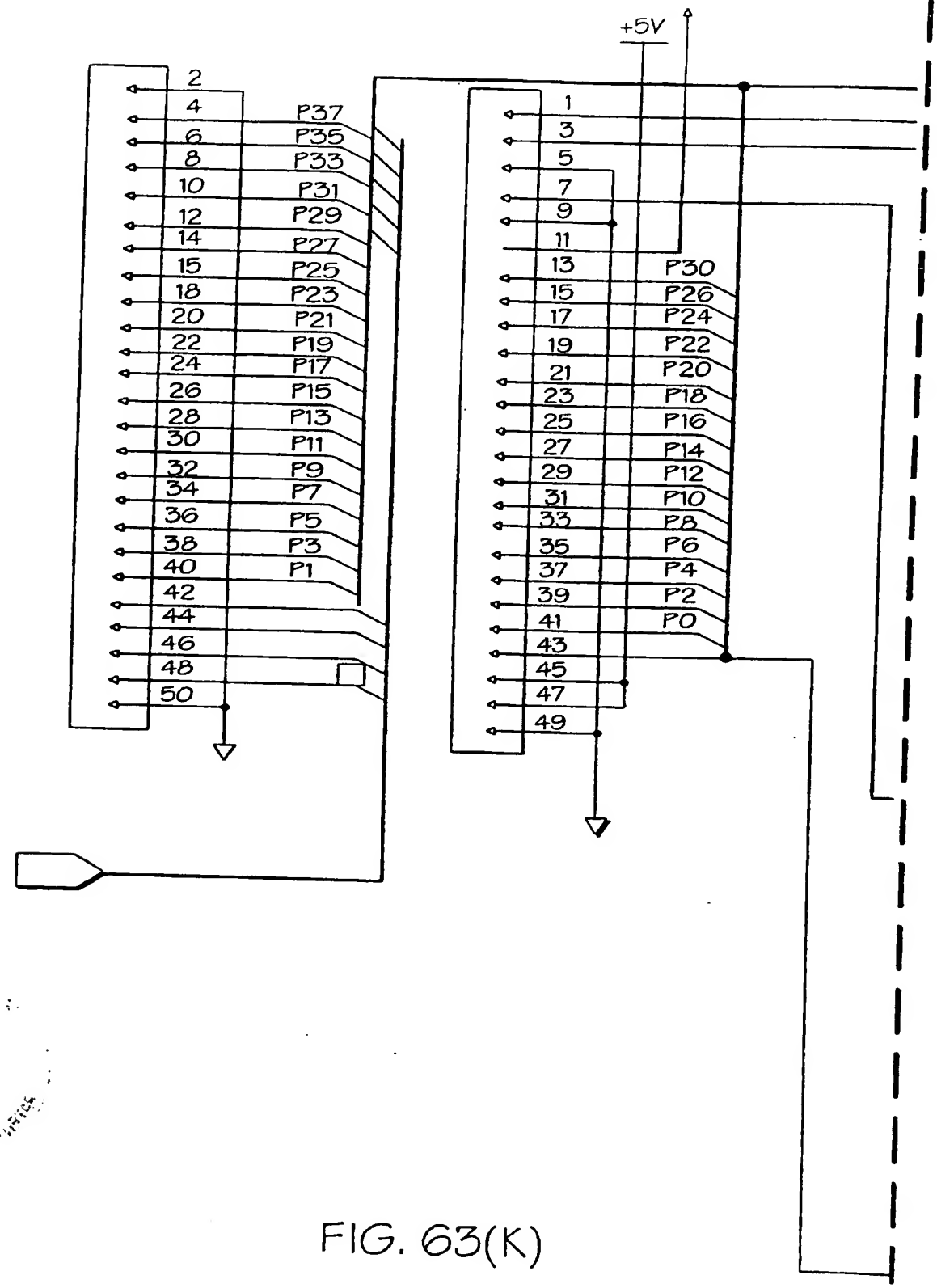

+5V
2
4
6
8
10
12
14
15
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
P37
P35
P33
P31
P29
P27
P25
P23
P21
P19
P17
P15
P13
P11
P9
P7
P5
P3
P1
1
3
5
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35
37
39
41
43
45
47
49
P30
P26
P24
P22
P20
P18
P16
P14
P12
P10
P8
P6
P4
P2
P0

FIG. 63(K)

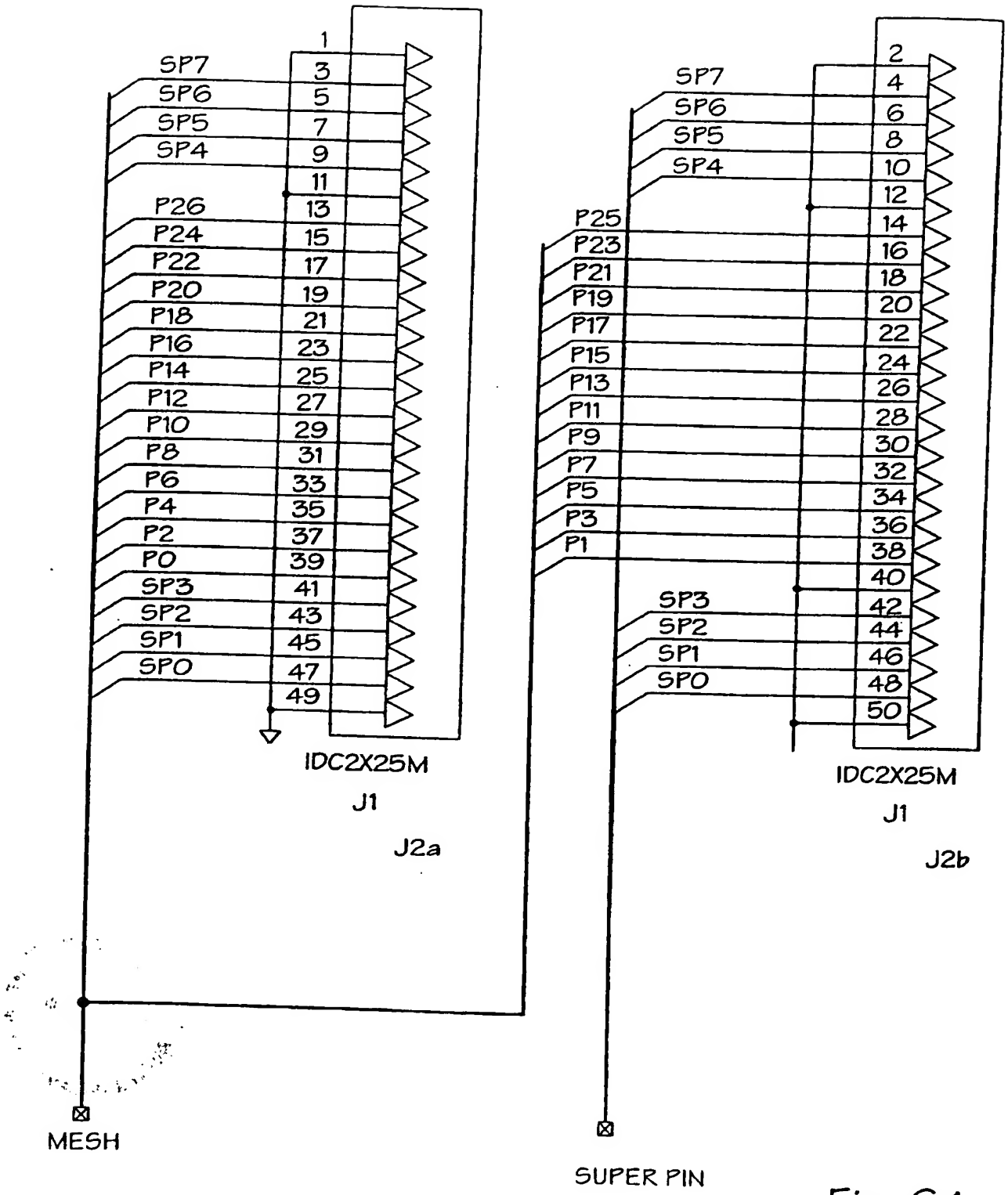
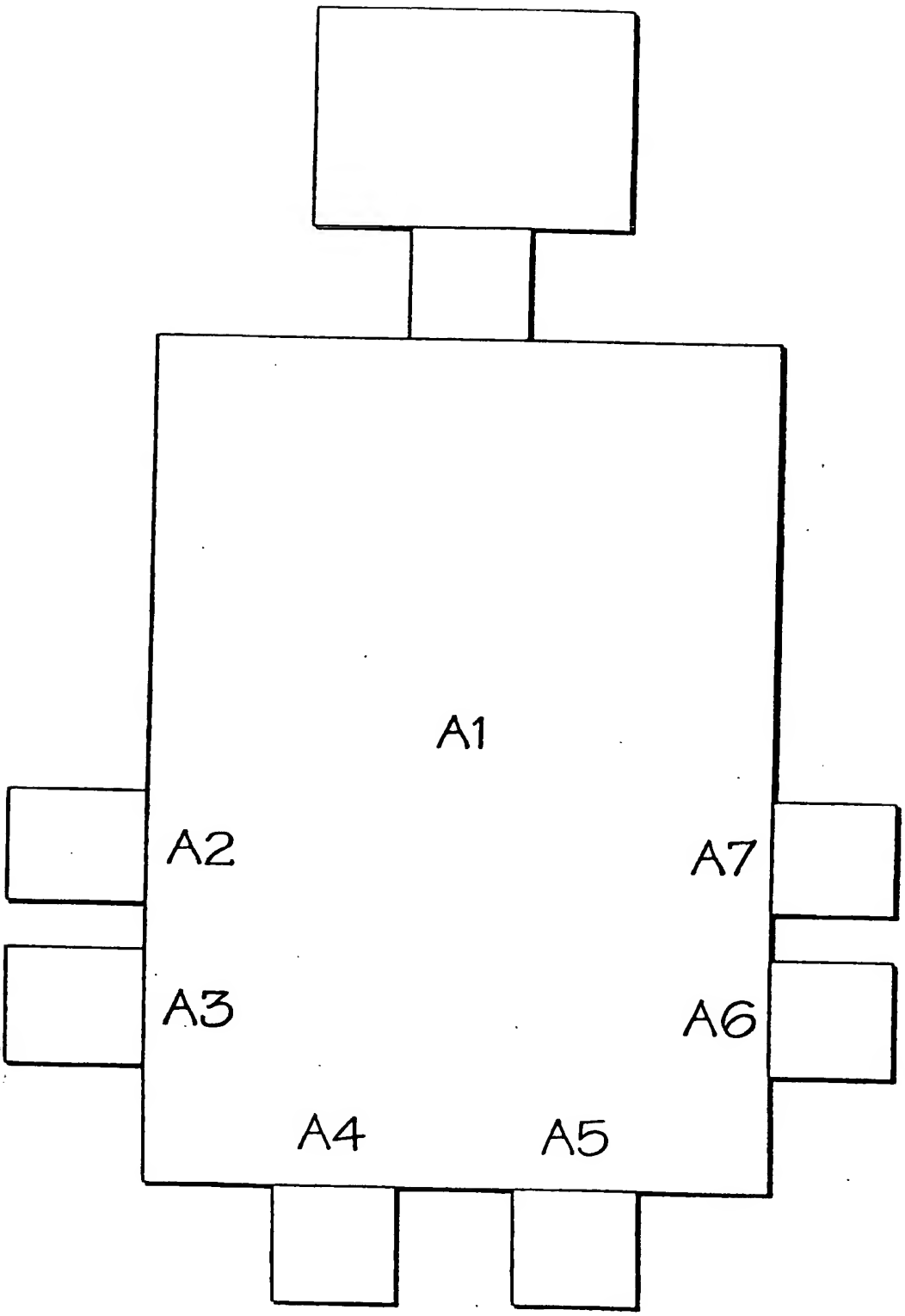

SP7
SP6
SP5
SP4
P26
P24
P22
P20
P18
P16
P14
P12
P10
P8
P6
P4
P2
P0
SP3
SP2
SP1
SP0
1
3
5
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35
37
39
41
43
45
47
49
IDC2X25M
J1
J2a
MESH
SP7
SP6
SP5
SP4
P25
P23
P21
P19
P17
P15
P13
P11
P9
P7
P5
P3
P1
SP3
SP2
SP1
SP0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
IDC2X25M
J1
J2b
SUPER PIN

Fig. 64

DOCUMENT 5980207



20120620090702

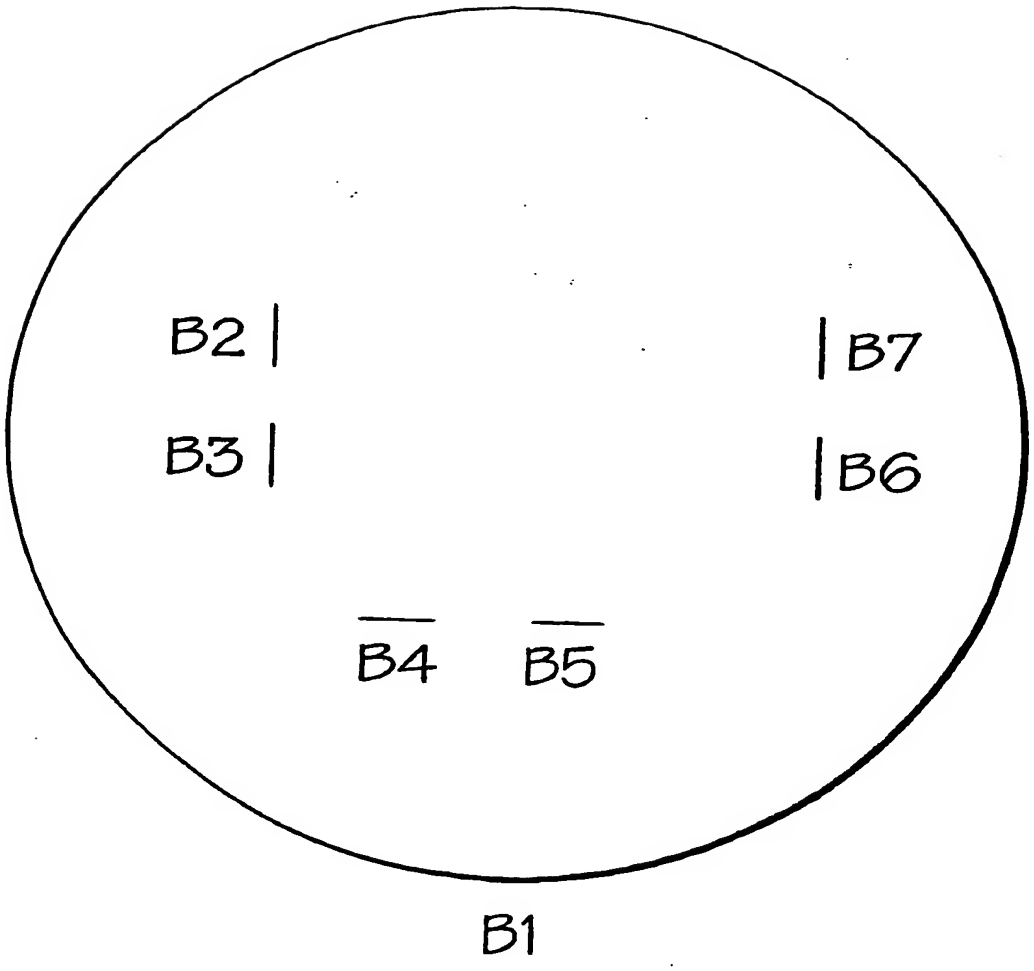
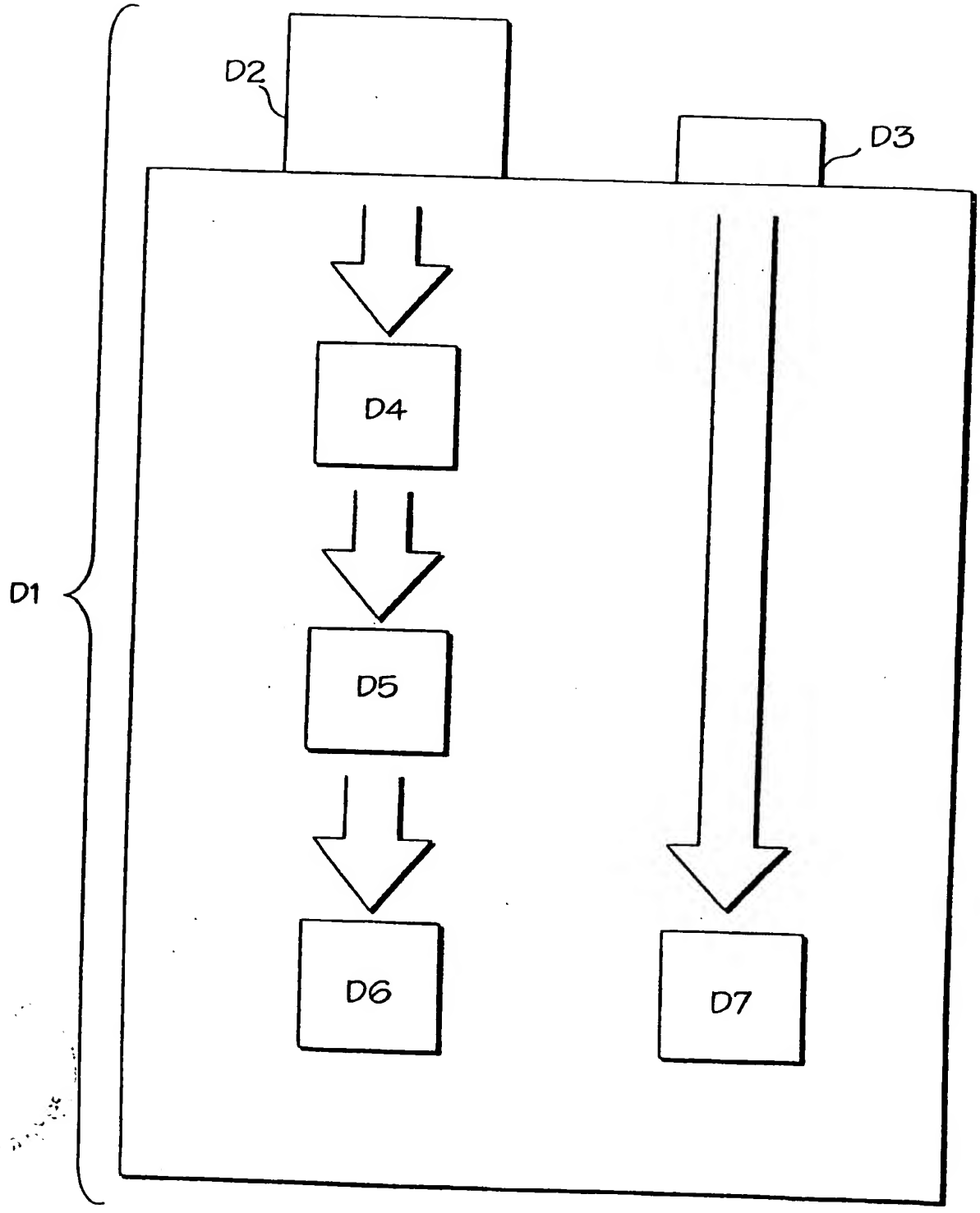


FIG. 66

20120926-2968-2004704

20150220



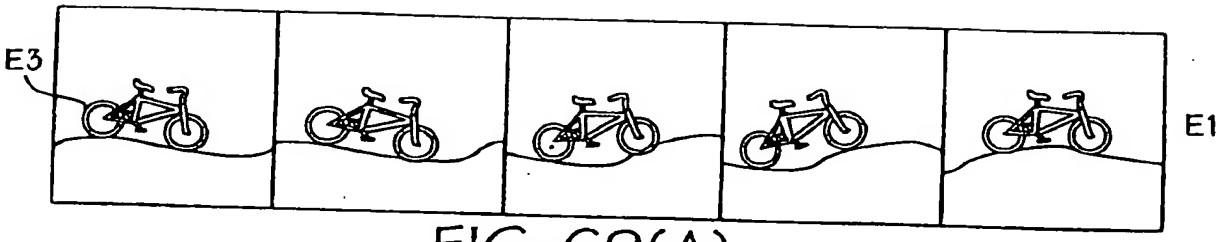


FIG. 69(A)

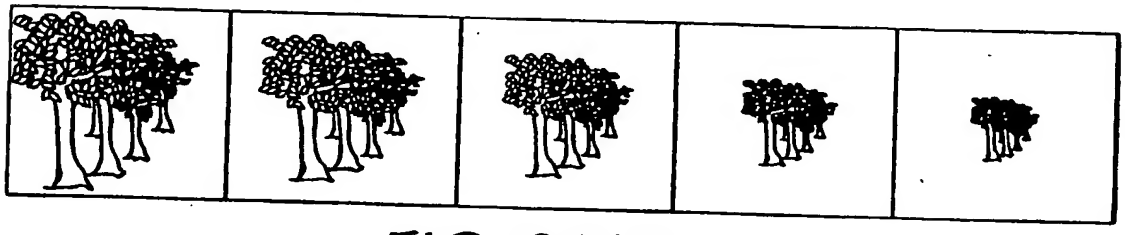


FIG. 69(B)

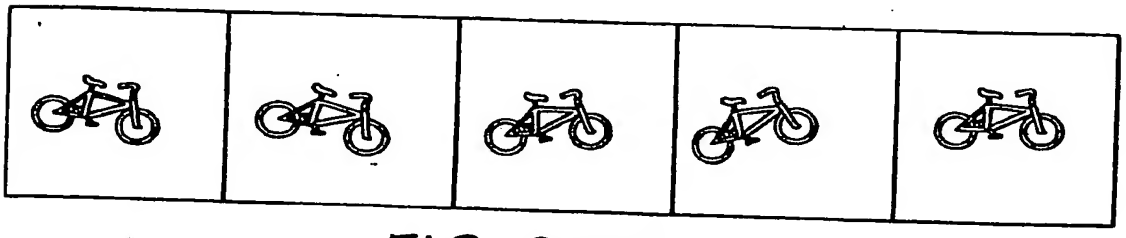


FIG. 69(C)

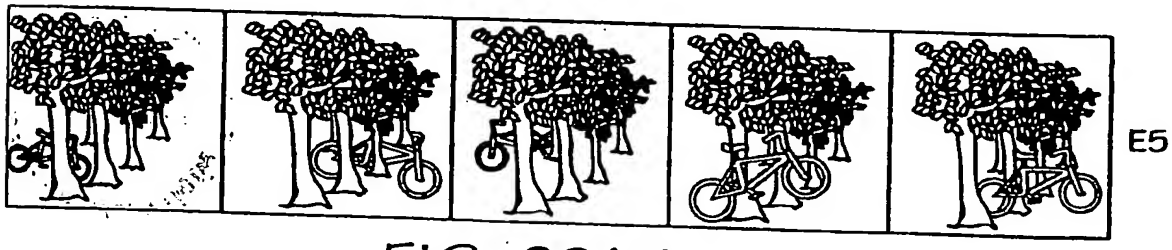


FIG. 69(D)